G 1241 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2016

Eighth Semester

Branch : Electronics and Communication Engineering/Applied Electronics and Instrumentation Engineering

VHDL Elective II (LA)

(Old Scheme—Prior to 2010 Admissions)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*

Each question carries 4 *marks.*

1. Define Entity and entity declaration.
2. Differentiate configuration and package declaration.
3. Write the syntax for If statement, wait statement.
4. Differentiate variable Assignment and signal assignment statements.
5. Explain Block statement with an example.
6. Define Generics used in VHDL.
7. Differentiate Direct Instantiation and Component Instantiation statements.
8. Write a short note on design Hierarchy in VHDL.
9. What is a signature ?
10. Define Aliases and Attributes.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*

Each full question carries 12 *marks.*

11. (a) Explain the various types of modelling used in VHDL with an example.

Or

(b) Explain the various types of operators used in VHDL.

Turn over

12. (a) Write the VHDL code to implement a 4 bit parallel adder using structural Modelling.

Or

(b) Write the VHDL code of implement a Half adder using 3 modelling styles.

13. (a) Explain configuration declaration with an example.

Or

(b) Write the VHDL code to implement a carry Look Ahead adder circuit.

14. (a) Explain package body and package declaration with an example.

Or

(b) Explain explicit and Implicit visibility with an example.

15. (a) Define attributes. What are the different types of attributes used in VHDL.

Or

(b) Write the VHDL code for modelling a pulse counter and clock Divider Circuit.

(5 × 12 = 60 marks)