G 1106

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Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2016

Seventh Semester

Branch : Electronics and Communication Engineering/Applied Electronics and Instrumentation Engineering

VLSI TECHNOLOGY (LA)

(Old Scheme—Prior to 2010 Admissions)

[Supplementary/Mercy Chance]

Time : Three Hours

Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries **4** *marks.*

1. What is drive-in diffusion ? How is its analytic solutions found ?
2. What is meant by etching ? Explain ion etching.
3. Explain dielectric isolation with a neat diagram.
4. [illegible]
5. Describe the area capacitance of layers.
6. Draw a monochrome stick notation for a CMOS inverter.
7. Draw the layout diagram for a two-input NOR gate.
8. Discuss double metal CMOS process design rules.
9. What is MESFET ? How is it different from MOSFET ?
10. What are the advantages of GaAs technology ?

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries **12** *marks.*

11. (a) Discuss in detail, the refining and growth of silicon crystals. (6 marks)

    (b) Describe ion implantation method and the distribution of implanted ions. (6 marks)

Or

12. (a) Describe the epitaxial growth process and state the differences between epitaxy and crystal growth. (6 marks)

(b) After a predisposition step, it is found that 5×10^{15} phosphorous atoms per cc are introduced in a p type silicon sample doped with 10^{16} acceptor atoms/cc. Calculate the junction depth when drive-in diffusion is performed at 1200° C. for two hours. $D = 2.5 \times 10^{-12}$ cm^2/s at 1200° C.

(6 marks)

13. With a neat cross-sectional view, explain the working of a nMOS enhancement type transistor. Explain the differences in fabrication between the enhancement and depletion type MOS.

Or

14. (a) Derive the threshold voltage for an ideal nMOS transistor without body effect. Discuss the factors affecting the threshold voltage ?

(8 marks)

(b) What is thermal feedback ? What are its effects on monolithic IC ? (4 marks)

15. With necessary labelled sketches, describe the "twin-tub" CMOS fabrication in detail.

Or

16. (a) Explain how latch-up condition may be induced in a well-based CMOS fabrication.

(7 marks)

(b) Draw and discuss the graph of latch-up current versus voltage. What are the remedies for latch-up problem ?

(5 marks)

17. (a) Discuss the layout generation using cell hierarchy. Explain the term "Regularity".

(6 marks)

(b) Discus the λ-based design rules as applied to nMOS, pMOS and cMOS transistors.

(6 marks)

Or

18. Draw neatly the stick diagram and mask layout for a 4-bit shift register.

19. Explain the significance and effects of sub-micron CMOS technology. What are its merits ?

Or

20. With neat sketches, explain the fabrication steps in a GaAs transistor.

(5 × 12 = 60 marks)