G 1298

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Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2016

Seventh Semester

Branch : Electronics and Communication Engineering

EC 010 701—VLSI DESIGN (EC)

(New Scheme—2010 Admission onwards)

[Improvement/Supplementary]

Time : Three Hours

Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. Mention three thermal oxidation and their oxidation species.
2. Draw the cross-section schematic of an integrated JFET and explain its regions.
3. Compare bipolar technology with CMOS technology.
4. What are the informations conveyed by stick diagrams ?
5. Why GaAs technology is preferred to silicon technology in the fabrication of LED ?

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Explain dry oxidation. Distinguish between wet oxidation.
7. Compare Dielectric Isolation (DI) and wafer bonding approach for forming SOI.
8. Explain Latch up problem in CMOS fabrication. How to reduce them ?
9. Draw the circuit of BiCMOS inverter.
10. What is MESFET ? How is it different from MOSFT ?

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each question carries 12 *marks.*

11. With neat sketches, explain the optical lithography process, at each step clearly.

Or

12. With neat diagrams, explain (i) Patterning ; (ii) wire bonding ; and (iii) Packaging.

Turn over

13. (a) With necessary diagrams, explain Schottky contacts and their properties. (6 marks)

(b) Explain the shallow trench isolation used for CMOS, with the help of neat sketches. (6 marks)

Or

14. What are IC cross-overs ? How cross-over in IC is managed ? How does bias help in this regard ?

15. Realise the logic diagram of the function $Y = A \oplus B$ using CMOS logic family. Draw its stick diagram and layout for the same.

Or

16. Describe a transmission gate. What are the advantages and disadvantages of using transmission gate for implementing the logic ? Also develop a 2-input CMOS multiplexer using transmission gates.

17. Sketch a D latch circuit using CMOS logic. With respect to a clocked D register, with the help of waveforms define hold time and set up time. Also define clock skew.

Or

18. Describe the circuit of a two-input NAND gate using BiCMOS technology. What are its merits compared to the other logic family types ?

19. (a) Describe a typical PLA architecture. (6 marks)

(b) Explain any two methods of programming a PLA. (6 marks)

Or

20. Draw and explain the structure of a metal gate depletion mode MESFET. Discuss the fabrication steps with necessary sketches.

[5 × 12 = 60 marks]