G 1261 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2015

Sixth Semester

Branch : Electronics and Communication Engineering

EC 010 606 L03—HIGH SPEED DIGITAL DESIGN (Elective I) (EC)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. What are the advantages of high speed digital design ?
2. What is cross-talk ? Why point-to-point wiring generates cross-talk ?
3. Define propagation delay ? How it is related to series inductance per unit length and its parallel capacitance per unit length ?
4. What is meant by inductance of vias ?
5. Explain clock jitter.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Explain the method of estimating decay time.
7. Explain cross talk in cross-talk in cross-hatched ground planes.
8. Define attenuation and characteristic impedance. Give a good model for transmission lines operated in their low-loss region.
9. What is meant by end termination ? Describe various methods used for end termination.
10. Sketch the timing analysis showing clock skew and explain.

(5 × 5 = 25 marks)

Turn over

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Explain power measurement techniques in high speed logic circuits.

Or

12. Discuss different types of reactive components which will affect for digital signal transmission. Derive equations for reactance in terms of rise time.

13. (a) Discuss the effect of self inductance, signal pickup and loading effects of probes. (8 marks)

(b) Why the point-to-point wiring generates cross-talk ? Explain. (4 marks)

Or

14. (a) Explain the rise time and bandwidth of oscilloscope with the help of neat figures and expressions. (6 marks)

(b) Discuss near and far and cross-talks. (6 marks)

15. Explain line impedance and propagation delay in transmission lines. Derive expression for both.

Or

16. Explain the following transmission line cases with neat sketches and expressions :

(a) Unterminated line with low source impedance. (4 marks)

(b) Capacitive loads connected in the middle of the line. (8 marks)

17. Explain clearly the factors that should be considered while selecting a terminating resistance ?

Or

18. (a) Discuss the return current and its relation to Vias. (8 marks)

(b) Explain the mechanical properties of Vias. (4 marks)

19. (a) What is clock skew ? Explain the methods to reduce clock skew. (8 marks)

(b) What is common path noise voltage ? Explain. (4 marks)

Or

20. (a) Discuss different clock delay adjustment methods for reducing the clock skew. (8 marks)

(b) Explain the significance of stable reference voltage. (4 marks)

[5 × 12 = 60 marks]