G 423

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Reg. No.....

Name.....

# **B.TECH. DEGREE EXAMINATION, MAY 2014**

## Sixth Semester

Branch: Electronics and Communication Engineering

EC 010 606 L03—HIGH SPEED DIGITAL DESIGN (Elective I) [EC]

(New Scheme-2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time: Three Hours

Maximum: 100 Marks

#### Part A

Answer all questions briefly. Each question carries 3 marks.

- 1. Discuss the relevance of mutual capacitance and mutual inductance in high speed circuits.
- Discuss how a probe load down a circuit.
- 3. Enumerate the thumb rules for calculating the resistance of rounded copper wires.
- 4. Enumerate the properties of an end terminated line.
- 5. Write a note on clock skew.

 $(5 \times 3 = 15 \text{ marks})$ 

#### Part B

Answer all questions.

Each question carries 5 marks.

- 6. With example, explain the active power dissipation in a totempole output circuit.
- 7. Write a note on shop-built 21:1 probe.
- 8. Write a note on reflections in transmission lines.
- 9. Write a note on inductance of vias.
- 10. Explain the different power system design rules.

 $(5 \times 5 = 25 \text{ marks})$ 

### Part C

Answer all questions.

Each full question carries 12 marks.

11. Explain the presence of different reactances in a high speed logic circuit.

Or

- 12. Explain the different circuit concepts to differentiate a low frequency and high frequency digital circuit. Explain how the step response is related to cross talk.
- 13. Explain how various operating margins are measured in digital systems.

Or

- 14. Explain metastability. How can it be measured? What are the cures for metastability?
- 15. Explain the different effects in a lossy transmission line. How does these affect the performance of the line?

Or

- 16. Explain the different factors that affect the attenuation in a transmission line.
- 17. Explain the factors to be considered in the selection of resistors in high speed circuits.

Or

- 18. Explain the factors that influence the design of vias. How is tradeoff achieved?
- 19. Explain the delay adjustments that are made in clock distribution of high speed ICs.

Or

20. Explain the selection of bypass capacitors. Discuss the different options for capacitors and dielectrics.

 $(5 \times 12 = 60 \text{ marks})$ 

