(Pages: 2)

Reg.	No
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Name.....

B.TECH. DEGREE EXAMINATION, MAY 2016

Fourth Semester

Branch: Electrical and Electronics Engineering

EE 010 405 - DIGITAL SYSTEMS AND COMPUTER ORGANISATION [EE]

(New Scheme - 2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time: Three Hours

Maximum: 100 Marks

Part A

Answer all questions.

Each question carries 3 marks.

- 1. Explain a combinational circuit.
- 2. What is a flip-flop?
- 3. Discuss the advantages of synchronous counters.
- 4 What is an Instruction cycle?
- 5. What is PCL?



 $(5 \times 3 = 15 \text{ marks})$

Part B

Answer all questions.
Each question carries 5 marks.

- 6. State and explain De-Morgan's Theorem.
- 7. Explain Sequential Circuits.
- 8. Draw a ring counter and explain its operation.
- 9. Explain Carry Look Ahead Adder and discuss its advantages.
- 10. Illustrate the advantages of a Dynamic RAM.

 $(5 \times 5 = 25 \text{ marks})$

Part C

Answer all questions.

Each full question carries 12 marks.

- 11. (a) Explain 8:1 MUX with a neat schematic diagram.
 - (b) Draw a BCD to 7 segment decoder.

(6 + 6 = 12 marks)

- 12. (a) Explain CMOS, NAND and NOR gate.
 - (b) Discuss the characteristic features of CMOS logic family.

(6' + 6 = 12 marks)

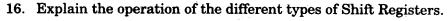
- 13. (a) What is Race around condition? How is it avoided?
 - (b) Explain the operation of Master Slave JK Flip-flop using gates with a neat figure.

(3 + 9 = 12 marks)

Or

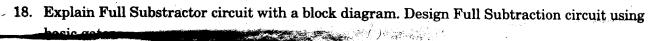
- 14. Design a Mod 12 Ripple Counter and explain.
- 15. Design a Mod 7 synchronous counter.

Or



17. Explain the Processor Bus Structure.

Or



- 19. (a) Explain the Memory Hierarchy.
 - (b) Write technical notes on the internal organisation of ROM.

(6 + 6 = 12 marks)

Or

- 20. (a) What are Buses?
 - (b) Explain the standard IO interfaces briefly.

(3 + 9 = 12 marks)

 $[5 \times 12 = 60 \text{ marks}]$