G 1612 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2016

Fourth Semester

Branch : Computer Science and Engineering

INTEGRATED CIRCUITS (R)

(Old Scheme—Prior to 2010 Admissions)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 *marks.*

1. Why ECL is operating at highest speed ?
2. What is tristate logic ? What are its applications ?
3. Differentiate between static and dynamic RAM.
4. What is CPLD ? Explain its applications.
5. For a ramp type ADC, f_c = 2 MHz, V_T = 2 mV, DAC has full-scale output of 12.70 V with 8 bit input.
6. Why parallel comparator type ADC is the fastest ? What are its drawbacks ?
7. Define CMRR and suggest methods to improve the same.
8. Draw the equivlent circuit of an op-amp and identify the parameters.
9. For an op-amp integrator circuit, 4 sin 1000 t is applied as input. If R = 200 MΩ, C = 0.01 μF, determine the value of the output voltage.
10. Sketch the output waveforms, if a square wave input is appiled to op-amp differentiator circuit. R = 100 Ω, C = 0.01 μF. Frequency of the square wave is 100 Hz.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. (a) Draw a CMOS circuit to realize $f = (a + b)\,\bar{c}$. (6 marks)

    (b) Sketch and explain a two-input AND gate of ECL family. (6 marks)

Or

Turn over

12. (a) For a logic gate, explain fan-in, fan-out, sinking and sourcing currents. (6 marks)

(b) Calculate the noise margin of a TTL standard gate. (6 marks)

13. With neat circuit diagrams, explain the static and dynamic RAM cells and show how 0 and 1 can be written and read.

Or

14. Implement the following function using 3 × 4 × 2 PLA with both true and complemented outputs. Write PLA table :

$f_1 = \Sigma m\ (0, 1, 3, 5)$

$f_2 = \Sigma m\ (0, 2, 3, 4)$.

15. With a neat circuit diagram, explain the working of a successive approximation type ADC. Illustrate with an example.

Or

16. Draw the circuit diagram of a 4 bit ladder type DAC and explain how the conversion is taking place. Derive the formula used.

17. Define and explain the following parameters of an op-amp. Give the values for ideal and practical cases :

(i) Input offset current. (ii) Input bias current.

(iii) Slew rate. (iv) PSRR.

Or

18. Explain the type of feedback in non-inverting amplifier cicuit of op-amp. Derive expressions for its A_{vf}, R_{if} and R_{of}.

19. With necessary waveforms and circuit diagram, explain the circuit of a square wave generator using op-amp. Derive expression for its frequency.

Or

20. With an integrator and regenerative comparator, assemble a circuit which can generate square and triangular waveforms. Derive expressions for the frequency and sweep amplitude.

[5 × 12 = 60 marks]