J 569 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Fourth Semester

Branch : Computer Science and Engineering

INTEGRATED CIRCUITS (R)

(Old Scheme—Prior to 2010 Admissions)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 *marks.*

1. List four commonly used series of TTL and mention their specialities.
2. What are the two advantages of using the wired AND connection ?
3. Explain, why negative edge triggered JK flip-flops are used in TTL families.
4. What are the RAM timing parameters that will determine its operating speed ?
5. A 16-bit DAC has an output of voltage range from 0 to 2.55 volt. Calculate the resolution of the system.
6. An 8-bit ADC accepts an input voltage signal of range 0 to 12 V. What is the minimum value of the input voltage required to generate a change of 1 LSB.
7. The output voltage of a certain op-amp circuit changes by 10 Volt in 3μS. Calculate its slew rate.
8. Draw the circuit diagram of a scale changer using op-amp and write the expression for its output voltage.
9. What is the principle of an op-amp differentiator ? What are its drawbacks ?
10. Draw the circuit diagram of an op-amp astable multivibrator to generate f_0 = 1.8 kHz.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Draw the circuit diagram of a 3-input TTL NAND gate which uses a totem pole output and explain its working. Verify how the circuit satisfies the truth table.

Or

12. Draw the circuit of a 4-input ECL OR gate and explain its working. Give its important features, compared to CMOS and TTL families.

Turn over

13. How many RAM chips will be required to build a 4K byte RAM memory if you are provided with nibble organized RAM chips each of capacity 4K bits ? Explain with necessary diagrams.

Or

14. Draw the internal construction of PLA having three inputs, three product terms and two outputs. Show how A $(x, y, z) = \Sigma m\ (1, 3, 5, 7)$.

15. For a 4 bit R-2R ladder DAC, assume that the full scale voltage is 10 V. Calculate the step change in output voltage when the input changes from 1001 to 1110. Explain with a circuit diagram.

Or

16. With a neat block diagram, explain the counter type ADC. Explain its merits.

17. Why do offset current and offset voltage exist in an op-amp ? What are the various ways of minimising them ? Explain with necessary circuit diagrams.

Or

18. (a) What is the virtual short concept in op-amp circuits ? What are the conditions to have virtual short ? Explain.

(6 marks)

(b) The output of an op-amp voltage follower is a triangular wave with 6V peak to peak voltage amplitude and frequency 2 MHz for a square wave input of frequency 2 MHz and 8V peak to peak amplitude. What is the slew rate of the op-amp ?

(6 marks)

19. With the help of neat circuit diagram, explain the working of a three-input non-inverting summer. Derive expression for its output voltage.

Or

20. Draw the circuit diagram of a sweep generator using op-amp with necessary waveforms explain its working. Design the circuit to generate a linear sweep ± 6V amplitude, 18.72 mS trace and 1.28 mS retrace period.

[5 × 12 = 60 marks]