F 3141 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Third Semester

Branch : Computer Science and Engineering

CS 010 304—COMPUTER ORGANISATION (CS)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 3 *marks.*

1. Suggest any one technique and briefly explain the same, to speed up the multiplication operation.
2. Write a note on floating point number representation.
3. What is microinstruction ? Write the format of microinstruction.
4. State two techniques to reduce cache miss penalty.
5. Differentiate between logical address and physical address.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Give steps for performing non-restoring division.
7. Describe how floating point multiplication can be carried out in a computer.
8. Explain micro-instruction sequencing with next address field.
9. With a neat block diagram, show how the performance of memory can be improved in interleaved organization of multiple memory modules.
10. Explain how a virtual address is mapped to physical address using page table.

(5 × 5 = 25 marks)

Turn over

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Multiply the following pair of signed 2's complement numbers using the Booth algorithm :

    A = 01101011 (Multiplicand)

    B = 10110010 (Multiplier)

Or

12. (a) Illustrate with an example the algorithm for restoring division. (6 marks)

    (b) With necessary diagrams, describe the working of a 4-bit carry look-ahead adder. (6 marks)

13. With necessary flow-charts, explain how floating point addition and multiplication are performed in a computer.

Or

14. Construct a 32-bit ALU from 1 bit ALU and explain how it performs various logical operations.

15. Design a microprogrammed and also hardwired control unit for bit pair multiplication scheme. Give the data path and control path with binary listing of the microprogram.

Or

16. (a) What are the different schemes followed in optimizing the control memory in microprogram control ?

    (6 marks)

    (b) Compare hardwired and microprogrammed approaches in the design of control units.

    (6 marks)

17. Organize the subfields of MAR to realize a block set associately mapped Cache-Main storage hierarchical memory with MS capacity of 16K pages of 16 word each and cache capacity of 256 pages divided into sets, each set having 8 pages.

Or

18. What are the placement policies and replacement policies in memory hierarchy ? Explain the common placement and replacement policies present in memory allocation.

19. What is memory paging ? Explain the paging registers, page directory and page table with neat diagrams.

Or

20. (a) Explain how the translation buffers speed up logical address generation. (7 marks)

    (b) What is TLB miss ? How it is handled ? (5 marks)

[5 × 12 = 60 marks]