F 3096 (Pages : 3) Reg. No.....

Name.....

SAINTGITS COLLEGE OF ENGINEERING LIBRARY KOTTAYAM

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Third Semester

Branch : Computer Science and Engineering/Information Technology

SOLID STATE ELECTRONICS (R, T)

(Prior to 2010 Admissions—Old Scheme)

(Supplementary/Mercy Chance)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 4 marks.

1. Define d.c. load line and Q-point.
2. Draw the circuit and explain the emitter follower with capacitor load.
3. With neat circuit diagram, explain self biasing circuit for *n*-channel JFET.
4. Why a FET is known as unipolar device ? How do you compare this device with BJT ?
5. Find the frequency of the oscillations of transistorised Colpits oscillator having tank circuit parameters as C_1 = 150 pF, C_2 = 1.5 nF and L = 50 μH.
6. Explain how oscillations are initiated and later sustained in an oscillator circuit.
7. Draw the input and output waveforms of a low pass RC circuit to a pulse input.
8. What is commutating capacitor ? Explain its function in a multivibrator circuit.
9. What are the various types of IC voltage regulators ? Explain the operation of any *one* IC voltage regulator.
10. Explain the differences between a TRIAC and thyristor. Enlist the applications of TRIAC.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each question carries 12 marks.

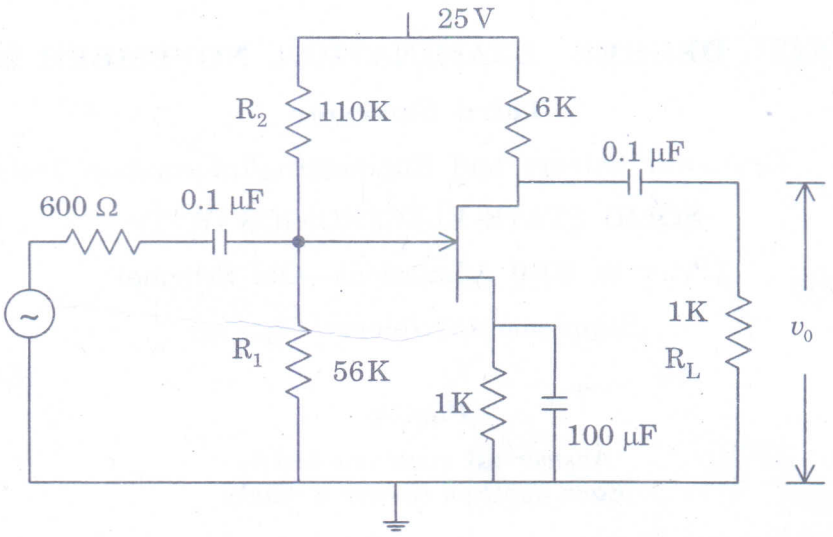
11. For the base bias circuit, (a) R_B = 150 kΩ and ; (b) R_B = 100 kΩ. Calculate I_B, I_C and V_{CE} if V_{CC} = 12 volt, R_C = 1.1 kΩ and β = 100. Also identify the operating regions of the transistor.

Or

12. Draw the Darlington pair circuit and derive its R_i, A_i, A_v and R_o.

Turn over

13. For the JFET amplifier circuit shown below :



g_m = 2.5 mS, r_d = 200 $k\Omega$, C_{gs} = 12 pF, C_{gd} = 2pF $R_1//R_2$ = 0.1 M, $C_W + C_L$ = 10 pF

(i) Draw the linear circuit for midfrequencies and calculate the midfrequency gain.

(ii) Determine the low frequency cut-offs caused by the input and output circuits. Which one of these is the low frequency cut-off of the complete frequency response ?

(iii) Determine the upper cut-offs caused by input and output circuits. Which one of these is the high frequency cut-off of the complete frequency response ?

Or

14. With neat diagrams explain the construction of an enhancement type p-channel MOSFET. Draw and explain its static characteristics. How is the threshold voltage of the MOS transistor adjusted ?

15. In a transistorised Hartley oscillator the two inductances are 2 mH and 20 μH while the frequency is to be changed from 950 KHz to 2050 KHz. Calculate the range over which the capacitor is to be varied. Draw the circuit and explain how sine waves are produced in it ?

Or

16. With neat circuit diagram, explain how sine was are produced in a transistor Wienbridge oscillator. Compare and contrast it with RC phase shift oscillator.

17. Draw the circuit diagram of astable multivibrator using transistors. Prove that the expression for the period of oscillation is 2T log 2, taking into account the $V_{CE_{sat}}$, $V_{BE_{sat}}$ and the cut-in voltage of the transistor.

Or

18. With a neat circuit diagram, describe the working of a transistorised Bootstrap time base generator. Explain clearly, the quiescent conditions, the formation of sweep, the retrace interval and the recovery process.

19. Explain the voltage adjustment provided by LM 317. Explain a circuit using LM 317 to obtain V_0 from 5V to 12 V, I_0 = 1 Amp. Design your circuit diagram.

Or

20. With a neat constructional diagram, explain the working of SCR. Explain its VI characteristics and describe how controlled rectification can be achieved ?

(5 × 12 = 60 marks)

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