F 3121 (Pages : 3) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Third Semester

Branch : Computer Science and Engineering

LOGIC SYSTEM DESIGN (R)

(Prior to 2010 Admissions—Old Scheme)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 4 *marks.*

1. Convert the following hexadecimal numbers into decimal and binary numbers :—
   (i) ECE ; (ii) 123 ;
   (iii) FACE ; (iv) 9A5.
2. Express the following decimals in Gray code form :—
   (i) 16 ;
   (ii) 1965.
3. Simplify using Boolean laws :
   (i) $AB + A(B + C) + B(B + C)$;
   (ii) $\overline{A} \oplus \overline{A + B}$.
4. Draw and explain how the basic gates can be realised using NAND gates.
5. List four different applications of flip-flops.
6. Show, with diagrams, how JK flip-flop can be converted as :
   (i) D-flop and ;
   (ii) T-flip-flop.
7. Write the truth table of a full subtractor and list its applications.
8. What is meant by look ahead carry adder ? What are its advantages ?
9. Why are shift registers considered to be basic memory devices ? Explain.
10. Explain 4 bit Johnson counter, mention its applications.

(10 × 4 = 40 marks)

Turn over

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. What is the most important characteristics of Gray code ? Prepare a table showing the 4 bit Gray code. Explain the rule for conversion of binary numbers to Gray code and vice versa and draw logic gate circuit diagrams.

Or

12. (a) Convert the decimal 2013 to both BCD and ASCII codes. For ASCII, an odd parity bit is to be appended to the left.

    (b) Find the correct code if the received code is 101101010. There are 4 parity bits and odd parity is used.

13. (a) Using Boolean algebra simplify :

$$F = ABC + A\,\bar{B}\,\bar{C} + A\bar{B}\,C + AB\,\bar{C}$$

    (b) Using K-map simplify :

$$A\,\bar{B}\,\bar{C} + A\bar{B}\,D + \bar{A}BC + \bar{A}\,C\bar{D} + \bar{A}\,\bar{C}\,\bar{D}$$

Or

14. A corporation having 100 shares entitles the owner of each share to cast one vote at the shareholders meeting. Assume that A has 40 shares, B has 30 shares, C has 20 shares and D has 10 shares. A two-third majority is required to pass a resolution in a shareholders meeting. Each of these four men has a switch which he closes to vote YES and open to vote NO for his percentage of shares. When the resolution is passed the output, LED must be ON. Derive a truth table for the output function and deduce a minimal circuit for the same.

15. Design a mod-9 synchronous counter and draw its timing diagram.

Or

16. Explain SR flip-flop and JK flip-flop using NAND gates and truth tables. Explain the differences between them.

17. Design and draw the circuit of a 4 bit combinational circuit incrementer using four half adders and explain how it increments the member by 1.

Or

18. Draw the circuit to show how a full adder can be converted to a full-subtractor with the inclusion of an inverter circuit.

19. Design a 4 bit shift register with parallel load using D flip-flops. There are two control inputs : shift and load. When shift = 1, the content of the shift register is shifted by one position. New data is transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register does not change :

S_1	S_2	Operation of register
0	0	no change
0	1	complement of the four inputs
1	0	clear register to 0 (synchronous with the clock)
1	1	load parallel data.

Draw the circuit diagram.

Or

20. Data 10101101 is fed to 8 bit SISO shift register. Show the status of the registers at various clock pulses. Explain with the help of circuit diagram.

(5 × 12 = 60 marks)