Course code	Course name	L-T-P-Credits	Year of Introduction
AE467	CMOS CIRCUIT DESIGN	3-0-0-3	2016

Prerequisite: EC204 Analog integrated circuits

Course objectives

- To give ideas about basic amplifiers, current Mirrors and Differential Amplifiers
- To impart idea of static and switching characteristics of the CMOS Inverter
- To study the operation of pass transistor logic and transmission gates
- To analyse Operational Amplifiers on its design and stability factors
- To familiarise different types of Memory and its decoder Circuits

Syllabus

Review of single stage MOS Amplifiers - current Mirrors - Differential Amplifiers - CMOS Inverter - Sequential Logic Circuits- Different CMOS Flip flop - MOS Operational Amplifiers- Stability and frequency compensation in Op amps - Design of a two stage Op amp - CMOS Circuit and Logic Design - Arithmetic Circuits in CMOS VLSI - Low power design - Designing Memory and Array Structures- Designing Combinational Logic Gates in CMOS.

Expected outcome

- At the end of the semester students will be able to obtain comprehensive knowledge in CMOS Circuit Design.

Text Books

1. Douglas A. Pucknell and K. Eshragian., "*Basic VLSI Design*" 3 rd Edition. PHI, 2000.
2. John P. Uyemura, "*Introduction to VLSI Circuits and Systems*", John Wiley & Sons 2002
3. Kesshab K. Parhi, "VLSI DIGITAL SIGNAL PROCESSING SYSTEMS", John Wiley & Sons 2002
4. Neil. H.E. Weste and K. Eshragian, "*Principles of CMOS VLSI Design*". 2 nd Edition. Addison-Wesley , 2000.
5. R. Jacob Baker, Harry W. LI., & David K. Boyce., "*CMOS Circuit Design*", 3 rd Indian reprint, PHI, 2000.

References

1. Jan M. Rabaey and et al, "*DIGITAL INTEGRATED CIRCUITS*", Pearson Edn. Inc. 2003
2. Kang & Leblebigi "*CMOS Digital IC Circuit Analysis & Design*"- McGraw Hill, 2003
3. Weste and Eshraghian, "*Principles of CMOS VLSI design" Addison*-Wesley, 2002

Course Plan

Module	Contents	Hours	Semester Exam Marks
I	Review of single stage MOS Amplifiers CS, CD, CG and cascode Amplifiers . Design of current Mirrors, Wilson current mirrors and Widlar current mirrors. Band gap voltage reference Differential Amplifiers: MOS Load Current Source, Current Mirror, Cascade Load.	6	15%
II	CMOS Inverter-Static Characteristics, Derivation for VTH,	7	15%

	V IL and VIH Switching Characteristics and Calculation of delay times Sequential Logic Circuits- Different CMOS Flip flops Theory of operation and Circuits of Pass transistor Logic and transmission gate.		
FIRST INTERNAL EXAMINATION			
III	MOS Operational Amplifiers, Cascode and Folded Cascode opamps . Stability and frequency compensation in Op amps. Design of a two stage Op amp DRAM, SRAM, Sense Amplifiers, Design of Row and Column Decoders Flash Memory- NOR and NAND Flash Memory Cell	7	15%
IV	CMOS Circuit and Logic Design-CMOS Logic structures. Advanced techniques in CMOS Logic Circuits-Mirror circuits, Pseudo NMOS, Tri-state circuits, Clocked CMOS, Dynamic CMOS Logic circuits, Dual Rail Logic Networks.	7	15%
SECOND INTERNAL EXAMINATION			
V	Arithmetic Circuits in CMOS VLSI-Bit Adder Circuits, Ripple Carry Adder, Carry Look Ahead Adders, Other High speed adders-Multiplexer based fast binary adders, Multipliers-Parallel multiplier, Wallace Tree and Dadda multiplier, Low power design- Scaling Versus Power consumption, Power reduction techniques.	8	20%
VI	Designing Memory and Array Structures - Memory classification, Memory Core - Read Only Memories, Non-volatile Read Write Memories, Read Write Memories, Content - Addressable or Associative Memories, Memory Peripheral Circuits - Address Decoders, Sense Amplifiers, Designing Combinational Logic Gates in CMOS.	7	20%
END SEMESTER EXAMINATION			

QUESTION PAPER PATTERN:

Maximum Marks:100 Exam Duration: 3 Hours

Part A

Answer any two out of three questions uniformly covering Modules 1 and 2 together. Each question carries 15 marks and may have not more than four sub divisions.

(15 x 2 = 30 marks)

Part B

Answer any two out of three questions uniformly covering Modules 3 and 4 together. Each question carries 15 marks and may have not more than four sub divisions.

(15 x 2 = 30 marks)

Part C

Answer any two out of three questions uniformly covering Modules 5 and 6 together. Each question carries 15 marks and may have not more than four sub divisions.

(20 x 2 = 40 marks)