Course	Course name	L-T-P-	Year of
code		Credits	Introduction
AE461	ARM SYSTEM ARCHITECTURE	3-0-0-3	2016

Prerequisite : Nil Course objectives

• To introduce the concepts of embedded processors and ARM based development.

Syllabus

Embedded Computers - Embedded System Design - ARM Architecture - Instruction Set - ARM Processor - Assembly programming - Component Interfacing - ARM interfacing programs - Peripherals In ARM Processors - Peripherals and their control - ARM tools and Peripherals - Arm Procedure Call Standard - Example C program.

Expected outcome

• At the end of the semester students must be able to obtain comprehensive knowledge in embedded processors and ARM based system.

Text Books

- 1. Steve Furber, "ARM system on Chip Architecture", 2nd Edition, Addison Wesley Publishers, 2013
- 2. Wayne Wolf, "Computers as Components Principles of Embedded Computing System Design", Morgan Kaufman Publishers, 2001

Reference Books:

- 1. David Seal, "ARM Architecture Reference Manual", 2nd Edition, Addison Wesley Publishers, 2001
- 2. Frank Vahid and Tony. D.Givargis, "Embedded System Design A Unified Hardware/Software Introduction", John Wiley Sons, 2000.

	Cour <mark>se</mark> Plan					
Module	Contents	Hours	Semester Exam Marks			
I	Embedded Computers – Characteristics of Embedded Computing Applications—Challenges in Embedded Computing. Embedded System Design —Process Requirements – Specification	6	15%			
II	ARM Architecture: The ARM Instruction Set Architecture. Bus structure and the peripherals. Register set, Exception modes, Software Interrupt.	6	15%			
FIRST INTERNAL EXAMINATION						
Ш	ARM Processor – Memory organization and processor initialization [start up code]. Load store instruction set. Assembly programming using Assemblers, Linkers, Loaders and Debuggers. Component Interfacing – Designing with Microprocessor Development and Debugging – Design Example Alarm Clock	8	15%			
IV	ARM interfacing programs: GPIO, Timers, Counters, PWM, ADC. Application coding examples: Measurement and control of time, frequency velocity acceleration, power	8	15%			

	control and touch monitoring			
	SECOND INTERNAL EXAMINATION			
V	Peripherals In ARM Processors: ARM / THUMB architecture. Program structure to Supervisor, Kernel, and User modes. Peripherals and their control: GPIO, Timers, Counters, PWM,	7	20%	
	ADC and serial communication channels.	N.A		
VI	ARM tools and Peripherals: ARM Development Environment, Arm Procedure Call Standard (APCS), Example C program.	7	20%	
	END SEMESTER EXAMINATION			

QUESTION PAPER PATTERN:

Maximum Marks: 100 Exam Duration: 3 Hours

Part A

Answer any two out of three questions uniformly covering Modules 1 and 2 together. Each question carries 15 marks and may have not more than four sub divisions.

 $(15 \times 2 = 30 \text{ marks})$

Part B

Answer any two out of three questions uniformly covering Modules 3 and 4 together. Each question carries 15 marks and may have not more than four sub divisions.

 $(15 \times 2 = 30 \text{ marks})$

Part C

Answer any two out of three questions uniformly covering Modules 5 and 6 together. Each question carries 15 marks and may have not more than four sub divisions.

(20 x 2 = 40 marks)