Course code	Course name	L-T-P-Credits	Year of Introduction
AE305	MICROPROCESSORS & MICROCONTROLLERS	3-0-0-3	2016

Prerequisite: Nil

Course Objective

- To expose the features of advanced microprocessors like 8086, 80386, and Pentium processors
- To introduce the architecture, programming, and interfacing of the microcontroller 8051

Syllabus

Intel 8086 - Assembler directives and operators - 8086 hardware design - Multi-processor configuration - Memory (RAM and ROM) interfacing - 8087 co-processor architecture and configuration - Introduction to 80386 - Superscalar architecture - 8051 Microcontroller - Assembly Language programming in 8051.

Expected outcome

At the end of the semester students will be

i. familiar with microprocessors and microcontrollers
ii. able to study the processor architecture, assembly language, memory management, interfacing etc.

Text Books

1. A K Ray and K M Bhurchandi, , Advanced Microprocessors and Peripherals, Tata McGraw Hill, 2006
2. D V Hall, Microprocessors and Interfacing: Programming and Hardware, 2nd ed., Tata McGraw Hill, 1999.
3. M A Mazidi and J. G. Mazidi, The 8051 Microcontroller and Embedded Systems, Pearson Education, Delhi, 2004
4. Ramani Kalpathi and Ganesh Raja, Microcontrollers and Applications, Pearson Education, 2010

Reference Books

1. B Brey, The Intel Microprocessors, 8086/8088, 80186, 80286, 80386 and 80486 architecture, Programming and interfacing, 6th ed., Prentice Hall of India, New Delhi, 2003
2. K J Ayala, The 8051 Microcontroller- Architecture, Programming and applications, Thomson Delmar Publishers Inc., India reprint Penram
3. Y C Liu and G A Gibson, Microcomputer system: The 8086/8088 family, 2nd ed., Prentice Hall of India, New Delhi, 1986

Course Plan

Module	Contents	Hours	Sem. Exam Marks
I	Intel 8086, format:, Assembler directives and operators, Assembly process, Linking and relocation, stacks, procedures, interrupt routines, macros.	7	15%
II	8086 hardware design - Bus structure, bus buffering and latching, system bus timing with diagram, Minimum and maximum mode configurations of 8086, Multi-processor configuration, 8087 co-processor architecture and configuration, Memory (RAM and ROM) interfacing, memory	8	15%

	address decoding.		
FIRST INTERNAL EXAMINATION			
III	8087 co-processor architecture and configuration, Memory (RAM and ROM) interfacing, memory address decoding	6	15%
IV	Introduction to 80386 – Memory management unit – Descriptors, selectors, description tables and TSS – Real and protected mode – Memory paging – Pentium processor -Special features of the Pentium processor – Branch prediction logic– Superscalar architecture, microprocessors - state of the art	7	15%
SECOND INTERNAL EXAMINATION			
V	8051 Microcontroller: Overview of 8051 family, architecture of 8051, Program counter, ROM space in 8051, data types and directives, flags and PSW register, register bank and stack, Addressing modes. Instruction set Arithmetic instructions JUMP, LOOP,CALL instructions, time delay generations.	7	20%
VI	Assembly Language programming in 8051 (some simple programs): programs using arithmetic and logic instructions, single bit instructions and programs, Timer/counter programming, 8051 serial communication programming, programming timer interrupts. Interfacing with Stepper motor, keyboard, DAC, external memory.	7	20%
END SEMESTER EXAMINATION			

QUESTION PAPER PATTERN:

Maximum Marks:100 Exam Duration: 3 Hours

Part A

Answer any two out of three questions uniformly covering Modules 1 and 2 together. Each question carries 15 marks and may have not more than four sub divisions.

(15 x 2 = 30 marks)

Part B

Answer any two out of three questions uniformly covering Modules 3 and 4 together. Each question carries 15 marks and may have not more than four sub divisions.

(15 x 2 = 30 marks)

Part C

Answer any two out of three questions uniformly covering Modules 5 and 6 together. Each question carries 15 marks and may have not more than four sub divisions.

(20 x 2 = 40 marks)