Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER B.TECH DEGREE EXAMINATION (R,S), DECEMBER 2023
COMPUTER SCIENCE AND ENGINEERING
(2020 SCHEME)

Course Code : 20CST203

Course Name: Logic System Design

Max. Marks : 100 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Perform the following base conversions a) $(A26E)_{16}$ to octal
   b) $(10110110110)_2$ to octal
2. Subtract 13 from 24 using 2's complement representation and 1's complement representation.
3. Simplify the expression: i) AB + ABC + ABC + BC
   ii) AB + A(B + C) + B(B + D)
4. Design a circuit using NAND gates for implementing EXCLUSIVE-OR function
5. Construct a 4X 16 decoder with two 3 X 8 decoders.
6. Design and implement a half subtractor.
7. Compare a T flip-flop with a D flip-flop.
8. Explain race around problem. How can it be eliminated?
9. Distinguish between a ring counter and Johnson counter.
10. What is programmable logic array? Where is it useful?

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Perform the following operations i) $(B242)_{HEX}$ +$(2CD6)_{HEX}$ ii) Add octal numbers 1257 and 7254 iii) BCD addition of 01110110 + 00110101 (9)
    .
    b) Find the 12 bit 2's complement representation of the following decimal numbers. (i) – 46 (ii) – 136 (iii) - 210 (5)

OR

12. a) Perform the following base conversions: (i) $(110110.110)_2$ to octal (ii) $(425.2)_8$ to binary (iii) $(324.3)_5$ to binary (9)
    b) Subtract 145 from 726 assuming the numbers are i) octal
    ii) hexadecimal (5)

MODULE II

13. a) Show that any digital circuit can be implemented using any universal gate (6)
    b) Simplify the Boolean function F(a,b,c,d) : (0,1,2,4,6,8,9,10,12,14,15) using K map (8)

OR

14. a) Express the following functions in a canonical form i) F= D+BC' ii) F: AB' +BC' (6)
    b) Simplify the Boolean function F(a,b,c,d) : (0,2,5,6,7,8,9,10,12,13,15) using tabulation method (8)

MODULE III

15. a) Design a code converter for converting a BCD to excess-3 code. (8)
    b) Design a 2 bit magnitude comparator. (6)

OR

16. a) Design a parallel adder/subtractor circuit with a logic diagram. (8)
    b) Design a 4x2 encoder circuit (6)

MODULE IV

17. a) Write the characteristics equation, excitation table of JK and D flipflop. (4)
    b) Design and implement a 4 bit binary synchronous down counter. (10)

OR

18. a) Explain asynchronous BCD counter. (4)
    b) Explain i) SR flip-flop ii) JK flip-flop iii) master-slave flip-flop with excitation table and characteristic equation (10)

MODULE V

19. a) With a neat diagram explain universal shift register. (7)
    b) Write algorithm for floating point addition and subtraction. (7)

OR

20. a) Explain the working of a 3 stage Johnson ring counter with a block diagram. (7)
    b) Write algorithm for addition and subtraction of two binary numbers in sign magnitude form. (7)

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