G 851 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Eighth Semester

Branch : Electronics and Communication Engineering / Applied Electronics and Instrumentation Engineering

VHDL (Elective II) (LA)

(Old Scheme—Supplementary/Mercy Chance—Prior to 2010 Admissions)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 4 *marks.*

1. What is enumeration data type?
2. Explain entity declarations using one example.
3. Write a VHDL program using dataflow modelling.
4. With a program example, explain "wait" statement.
5. Explain generics with an example.
6. What is incremental binding? Give an example.
7. What is operator overloading? Give an example.
8. Explain a type conversion function.
9. Write a short note on aliases with an example.
10. Give the properties of aggregate targets.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. With appropriate examples, explain all types of architectural bodies in VHDL.

Or

12. Describe the data objects in VHDL with suitable examples.
13. With necessary examples, explain "case" statement and "loop" statements.

Or

14. Explain with suitable examples, the different types of conditional statements that can be used in VHDL.

Turn over

15. Using generic, design a 4-bit down counter.

Or

16. Write description for an eight-to-one multiplexer with a 3-bit decoded input.

17. With necessary program examples, explain packages and libraries.

Or

18. Show the overloading function for the XOR operator and explain the program.

19. Write a test bench program for 8-bit register with asynchronous reset and load.

Or

20. Explain the design issues in a interacting state machine modelling.

(5 × 12 = 60 marks)