Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FIRST SEMESTER M.TECH DEGREE EXAMINATION (Regular), DECEMBER 2023

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: 21VE104-E

Course Name: ASIC Design and Verification

Max. Marks: 60 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Illustrate gate level modeling in verilog with an example.
2. Illustrate testbench structure in Verilog.
3. Differentiate Verilog and SystemVerilog.
4. Explain SystemVerilog Semaphore.
5. List the benefits of using UVM.
6. Explain the concept of Transaction Level Modelling.
7. Describe 'reporting' in UVM.
8. List out the advantages of UVM sequence.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. Implement a full subtractor using dataflow modelling in Verilog. (6)

OR

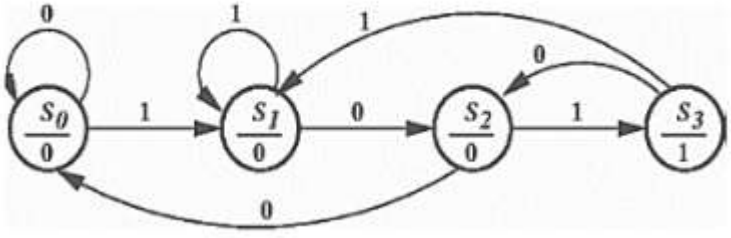
10. Implement the SOP Y=AC+BA'+AD in verilog using structural and gate level modeling. (6)

MODULE II

11. Illustrate the Verilog code for 4 bit ALU and its testbench using Verilog. (6)

OR

12. Implement the following state machine in Verilog. (6)



MODULE III

13. List SystemVerilog data types with suitable example. (6)

OR

14. Illustrate Arrays and Classes in SystemVerilog with suitable example. (6)

MODULE IV

15. Explain SV assertions in SystemVerilog with suitable examples (6)

OR

16. Illustrate Bus Functional Models in SystemVerilog. (6)

MODULE V

17. Describe the components of a Testbench (6)

OR

18. Discuss the possibility of user defined phase in UVM with an example. (6)

MODULE VI

19. Illustrate the process of DUT integration with testbench and running test cases in UVM. (6)

OR

20. Explain the connection and components of RAL with testbench. (6)

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