G 1311 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2015

Seventh Semester

Branch : Electronics and Communication Engineering/Applied Electronics and Instrumentation

VLSI TECHNOLOGY (L, A)

(Old Scheme—Prior to 2010 Admissions)

[Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 *marks.*

1. Explain the process of crystal growth.
2. Elaborate X-ray lithography process.
3. Discuss junction isolation and dielectric isolation.
4. List the difference between PMOS and NMOS fabrication process.
5. Decribe latchup problem in CMOS.
6. Write a brief note on scaling of MOS structures.
7. Using a diagram show the CMOS logic implementation using NOR.
8. Explain how power dissipation problems are handled in CMOS.
9. Discuss the principles specific to GaAs fabrication.
10. Explain the crystal structure of GaAs using diagrams.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each question carries 12 *marks.*

11. With neat diagram, explain electron beam and X-ray lithography.

Or

12. Discuss the various ways in which lithography can be performed.

13. Explain with relevance fig and steps of CMOS fabrication techniques.

Or

14. Discuss the fabrication of resistors in a region grown on a substrate.

Turn over

15. Elaborate with neat figure metal gate and silicon gate and its oxide isolation.

Or

16. Discuss the BiCMOS fabrication steps and the circuit design process.

17. With neat derivation derive dynamic power dissipation.

Or

18. Explain the working of a serial shifter and disuss its design.

19. With neat figure, explain sub-micron CMOS technology.

Or

20. Explain the chennelling effect and how it affects the fabrication process.

(5 × 12 = 60 marks)