G 1293 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2016

Seventh Semester

Branch : Applied Electronics and Instrumentation Engineering

AI 010 701—VLSI (AI)

(New Scheme—2010 Admission onwards)

[Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. State Fick's laws of diffusion.
2. List the steps involved in a subsystem design.
3. List the different types of isolation techniques.
4. What is latch-up in CMOS fabrication ?
5. Give reasons why GaAs technology is preferred in the fabrication of LED.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. How a *p*-type crystal is prepared using epitaxial growth ?
7. Describe λ based design rules for metals and pads.
8. Draw the layout of a junction isolated BJT.
9. Explain the salient features of Twin-tub process.
10. What is MESFET ? How is it different from MOSFET ?

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. What is fine line lithography ? Explain the process, with neat sketches of each step of IC fabrication, by the above method.

Or

Turn over

12. (a) With neat diagrams, explain MBE. (6 marks)

(b) Discuss the solution for predeposition and drive-in diffusion. (6 marks)

13. (a) Explain the λ rules for poly, diffusion layers, contacts and transistors. (6 marks)

(b) Draw the circuit, stick diagram and layout for a 2-input CMOS NAND gate. (6 marks)

Or

14. (a) What are FPGA ? Name the constituents of a generic FPGA ? Name two companies producing FPGA.

(3 marks)

(b) Draw a BicMOS NOR circuit with *npn* pull down and nMOS pull down and explain.

(9 marks)

15. What are IC cross-overs ? How cross-over in IC is managed ? How does bias help in this regard ?

Or

16. (a) With necessary diagrams, explain a shallow trench isolation for CMOS. (6 marks)

(b) Explain Schottky contacts and their properties. (6 marks)

17. Explain the design rules for CMSO n-well process.

Or

18. With neat sketches, explain the twin-tub CMOS process.

19. Draw the structure of metal gate depletion mode MESFET and explain.

Or

20. Explain the crystal structure and doping process in GaAs technology.

(5 × 12 = 60 marks)