

Register No.:

Name :

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SIXTH SEMESTER B.TECH DEGREE EXAMINATION (S), AUGUST 2023**ELECTRONICS AND COMMUNICATION ENGINEERING****(2020 SCHEME)****Course Code : 20ECT308****Course Name : Comprehensive Course Work****Max. Marks : 50****Duration : 75 Minutes****PART A****(Answer all questions. Each question carries 1 mark)**

- 1 The voltage gain of an amplifier is 100. A negative feedback is applied with $\beta=0.03$. The overall gain of the amplifier is

A. 70	B. 25
C. 99.97	D. 3
- 2 CE configuration is the most preferred transistor configuration when used as a switch because

A. It requires only one power supply	B. It requires low voltage or current for operating the switch
C. It is easily understood by everyone	D. It has small I_{CEO}
- 3 A Wien bridge oscillator uses Feedback

A. Only positive	B. Only negative
C. Both positive and negative	D. None of the above
- 4 The point of intersection of d.c. and a.c. load lines represents

A. Operating point	B. Current gain
C. Voltage gain	D. None of the above
- 5 An RC amplifier stage has a bandwidth of 500KHz. What will be the rise time of this amplifier stage?

A. $0.35\mu\text{s}$	B. $0.7\mu\text{s}$
C. $1\mu\text{s}$	D. $2\mu\text{s}$
- 6 The voltage gain of an amplifier without feedback and with negative feedback respectively is 100 and 20. The percentage of negative (β) would be

A. 4%	B. 5%
C. 20%	D. 80%
- 7 The product of which of the following gives the figure of merit of a logic family?

A. Gain and bandwidth	B. Propagation delay time and power dissipation
C. Fan-out and propagation delay time	D. Noise margin and power dissipation
- 8 For Emitter Coupled Logic (ECL), the switching speed is very high because

A. Negative logic is used	B. The transistors are not saturated when they are conducting
C. Multi emitter transistors are used	D. Low fan out
- 9 The 2's complement representation of -17 is

A. 100001	B. 101111
C. 110011	D. 101110
- 10 11001, 1001, and 111001 correspond to the 2's complement representation of which one of the following sets of numbers?

A. 25,9 and 57 respectively	B. -6,-6,and -6 respectively
C. -7,-7 and -7 respectively	D. -25,-9 and -57 respectively

- 11 The hexadecimal conversion of decimal number 227
A. A3 **B.** E3
C. CC **D.** C3
- 12 In 2's complement representation the number 11100101 represents the decimal number
A. +37 **B.** -31
C. +27 **D.** -27
- 13 Which one of the following circuits is used for converting a sine wave into a square wave?
A. Astable multi vibrators **B.** Mono stable multi vibrators
C. Bistable multi vibrators **D.** Schmitt trigger
- 14 The output frequency of the VCO can be changed by changing
A. External tuning resistor **B.** External tuning capacitor
C. Modulating input voltage **D.** All of the mentioned
- 15 A 1 μ s pulse can be stretched into a 1 ms pulse by using
A. A mono stable multi vibrator **B.** An astable multi vibrator
C. A bistable multi vibrator **D.** A JK flip flop
- 16 Which one of the following causes phase shift through an op-amp?
A. Internal RC circuits **B.** External RC circuits
C. Gain roll off of the internal transistor **D.** Negative feedback
- 17 How many bits will a D/A converter use so that its full scale output voltage is 5V and its resolution is at the most 10mV
A. 5 **B.** 7
C. 9 **D.** 11
- 18 In a 741 op-amp, there is 20dB/decade fall-off starting at a relatively low frequency. This is due to the
A. Applied load **B.** Internal compensation
C. Impedance of the source **D.** Power dissipation in the chip
- 19 Decimation is the process of
A. Retaining sequence values of $X_p[n]$ other than zeros **B.** Retaining all sequence values of $X_p[n]$
C. Dividing all sequence values by 10 **D.** Multiplying the sequence value by 10
- 20 For an N point FFT algorithm with $N=2^m$, which one of the following statement is true?
A. It is not possible to construct a signal flow graph with both input and output in normal order **B.** The number of butterflies in the m^{th} stage is N/m
C. In-place computation requires storage of only $2N$ node data **D.** Computation of a butterfly requires only one complex multiplication
- 21 Which of the following properties is correct for FIR (Finite Impulse Response) filters?
A. FIR filters are generally canonical **B.** FIR filters are not always stable
C. FIR filters require less memory than IIR filters **D.** FIR filter's linear phase realisation structure cannot be designed easily
- 22 If $x(n)$ and $X(k)$ are an N-point DFT pair, then $X(k+N)=?$
A. $X(-k)$ **B.** $-X(k)$
C. $X(k)$ **D.** None of the mentioned
- 23 The Chebyshev filters have
A. Flat pass band **B.** Flat stop band & Equiripple pass band
C. Tapering stop band **D.** Flat pass band & Tapering stop band

- 24 Which of the following methods are used to convert analog filter into digital filter?
A. Approximation of Derivatives **B.** Bilinear transformation
C. Impulse invariance **D.** All of the mentioned
- 25 A communication channel disturbed by Gaussian noise has a bandwidth of 6kHz and S/N ratio of 15. The maximum transmission rate that such a channel can support is
A. 2.4 kbits/sec **B.** 24 kbits/sec
C. 32 kbits/sec **D.** 48 kbits/sec
- 26 An audio signal, $15\sin(2\pi * 1500t)$ amplitude modulates $60\sin(2\pi * 1000t)$. The modulation index will be
A. 20% **B.** 50%
C. 25% **D.** 100%
- 27 In delta modulation, the slope overload distortion can be reduced by
A. Decreasing the step size **B.** Decreasing the granular noise
C. Decreasing the sampling rate **D.** Increasing the step size
- 28 When noise is passed through a narrow band filter, the output of filter should be?
A. triangular **B.** square
C. parabolic **D.** sinusoidal
- 29 The Nyquist sampling rate for the signal $s(t) = \frac{\sin(500\pi t)}{\pi t} * \frac{\sin(700\pi t)}{\pi t}$ is given by
A. 400Hz **B.** 600Hz
C. 1200Hz **D.** 1400Hz
- 30 A PLL can be used to demodulate
A. PAM signal **B.** PCM signal
C. FM signal **D.** DSB-SC signal

PART B

(Answer all questions. Each question carries 2 marks)

- 31 A certain regulator has a no-load voltage of 6 V and a full-load output of 5.82 V. What is the load regulation?
A. 3.09% **B.** 2.87 %
C. 2.72 % **D.** None of the above
- 32 The drain gate capacitance of a junction FET is 2pF. Assuming a common source voltage gain of 20, what is the input capacitance due to Miller effect?
A. 21pF **B.** 40pF
C. 42pF **D.** 10pF
- 33 Decimal 43 in hexadecimal and BCD number system is respectively..... and
A. B2 and 01000011 **B.** 2B and 01000011
C. 2B and 00110100 **D.** B2 and 01000100

