Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SIXTH SEMESTER B.TECH DEGREE EXAMINATION (S), AUGUST 2023
ELECTRONICS AND COMMUNICATION ENGINEERING
(2020 SCHEME)

Course Code : 20ECT304

Course Name: VLSI Circuit Design

Max. Marks : 100 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. State Moore's law in VLSI design.
2. List the advantages of System on Chip.
3. Realize an OR gate using CMOS logic.
4. What is pass transistor logic? Give an example.
5. Describe 'Precharge' and 'Evaluate' operations in dynamic logic circuits.
6. Draw the circuit diagram of a one-transistor dynamic RAM cell.
7. Write the expression for the worst-case delay of a square root carry select adder.
8. Calculate the delay of a 2*2 Array multiplier.
9. What is photolithography?
10. List any 3 Lambda based design rules.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Explain the ASIC design flow with the help of a diagram. (9)
    b) Distinguish between Full Custom and Semi-Custom ASIC. (5)

OR

12. a) What is FPGA? What are its applications? With a block diagram explain its internal architecture. (9)

b) Explain power consideration in ASIC. (5)

MODULE II

13. a) Explain about CMOS inverter and its VTC. (9)

b) Realize a NAND gate using nMOS logic and explain its operation. (5)

OR

14. a) Explain the transient characteristics of CMOS inverter. (7)

b) Implement 4:1 MUX using transmission gate and explain its operation. (7)

MODULE III

15. a) What is the "charge sharing" problem? Explain any one method with neat diagrams to overcome it. (8)

b) Draw and explain a NORA (NP-Domino) logic? (6)

OR

16. a) Draw the circuit diagram of a 6T CMOS SRAM cell. Briefly explain the read-and-write operations. (8)

b) Design a 4× 4 ROM array using NAND and explain its working. (6)

MODULE IV

17. a) Design of a full adder with not more than 28 transistors in standard CMOS logic. (8)

b) Explain the block diagram of a 16-bit carry-bypass adder. (6)

OR

18. a) Illustrate the principle of operation of a linear carry select adder. (7)

b) Design a 4x4 array multiplier and estimate the delay of the multiplier. (7)

MODULE V

19. a) With the help of a diagram explain the CZ process for crystal growth. (8)

b) Explain Electron beam lithography. (6)

OR

20. a) Explain the twin Well process in CMOS fabrication with neat sketches. (8)

b) Draw the layout diagrams for 2 input NAND gate. (6)

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