Register No.: ..... Name : .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SIXTH SEMESTER B.TECH DEGREE EXAMINATION (R), MAY 2023

ELECTRONICS AND COMMUNICATION ENGINEERING

(2020 SCHEME)

Course Code : 20ECT308

Course Name : Comprehensive Course Work

Max. Marks :50 **Duration : 75 Minutes**

PART A

(Answer all questions. Each question carries 1 mark)

1 For a full wave rectifier, with sinusoidal input and inductor as filter, ripple factor for maximum load current and minimum load current conditions are respectively

A. 0.1 and 1 **B.** 0.1 and 0.47

C. 0 and 0.47 **D.** 0 and 0.22

2 An amplifier has a power gain of 100. Its db gain is .....

A. 10dB **B.** 20dB

C. 40dB **D.** 0dB

3 The voltage gain of an amplifier is 100. A negative feedback is applied with β=0.03. The overall gain of the amplifier

A. 70 **B.** 25

C. 99.97 **D.** 3

4 The voltage gain of an amplifier without feedback and with negative feedback respectively is 100 and 20. The percentage of negative (β) would be

A. 4% **B.** 5%

C. 20% **D.** 80%

5 If V_{cc} =18V, voltage divider resistance $R_1 = 4.7K\Omega$ and $R_2 = 1500\Omega$, what is the base bias voltage ?

A. 8.70V **B.** 4.35V

C. 2.9V **D.** 0.70V

6 An oscillator employs ..... feedback

A. Positive **B.** Negative

C. Neither positive nor negative **D.** Data insufficient

7 A full adder can be made out of .....

A. two half adders B. two half adders and a OR gate

C. two half adders and a NOT gate D. three half adders

8 For Emitter Coupled Logic (ECL), the switching speed is very high because

A. Negative logic is used **B.** The transistors are not saturated when they are conducting

C. Multi emitter transistors are used **D.** Low fan out

9 The product of which of the following gives the figure of merit of a logic family?

A. Gain and bandwidth **B.** Propagation delay time and power dissipation

C. Fan-out and propagation delay time **D.** Noise margin and power dissipation

10 The 2's complement representation of -17 is

A. 100001 **B.** 101111

C. 110011 **D.** 101110

11 A digital circuit that can store only one bit is a

A. Register **B.** NOR gate

C. Flip-flop **D.** XOR gate

12 Which logic family is the fastest?

A. DTL **B.** CMOS

C. TTL **D.** ECL

13 For a given op-amp, CMRR=10^5 and differential gain= 10^5 .What is the common mode gain of the op-amp?

A. infinity **B.** 10^5

C. $2x10^5$ **D.** 1

14 In a circuit, if the open loop gain is 10^6 and output voltage is 10V, the differential voltage should be

A. 10 μv **B.** 0.1 v

C. 100 μv **D.** 1 μv

15 How many bits will a D/A converter use so that its full scale output voltage is 5V and its resolution is at the most 10mV

A. 5 **B.** 7

C. 9 **D.** 11

16 The large signal bandwidth of an op-amp is limited by its

A. CMRR **B.** Slew rate

C. Gain-bandwidth product **D.** Input impedance

17 A 1 μs pulse can be stretched into a 1 ms pulse by using

A. A mono stable multi vibrator **B.** An astable multi vibrator

C. A bistable multi vibrator **D.** A JK flip flop

18 Which one of the following circuits is used for converting a sine wave into a square wave?

A. Astable multi vibrators **B.** Mono stable multi vibrators

C. Bistable multi vibrators **D.** Schmitt trigger

19 For an N point FFT algorithm with N=2^m , which one of the following statement is true?

A. It is not possible to construct a signal flow graph with both input and output in normal order **B.** The number of butterflies in the m^{th} stage is N/m

C. In-place computation requires storage of only 2N node data **D.** Computation of a butterfly requires only one complex multiplication

20 The transformation technique in which there is one to one mapping from s-domain to z-domain is

A. Approximation of derivatives **B.** Impulse invariance method.

C. Bilinear transformation method **D.** Backward difference for the derivative

21 Which of the following methods are used to convert analog filter into digital filter?

A. Approximation of Derivatives **B.** Bilinear transformation

C. Impulse invariance **D.** All of the mentioned

22 What is the process of increasing the sampling rate by a factor I?

A. Sampling rate conversion **B.** Decimation

C. Interpolation **D.** None of the mentioned

23 A digital filter is said to be an IIR if:

A. It oscillates **B.** All its poles lies outside unit circle

C. Present output depends on previous output **D.** One or more denominator coefficient is zero

24 What is another term used for time scaling operation in digital signal processing?

A. Upsampling **B.** Downsampling

C. Convolution **D.** Quantisation

25 A communication channel disturbed by Gaussian noise has a bandwidth of 6kHz and S/N ratio of 15. The maximum transmission rate that such a channel can support is

A. 2.4 kbits/sec **B.** 24 kbits/sec

C. 32 kbits/sec **D.** 48 kbits/sec

26 If the modulating frequency of a carrier wave varies between 700Hz and 7KHz, find its bandwidth?

A. 10 KHz **B.** 23 KHz

C. 17.3 KHz **D.** 12.6 KHz

27 The minimum bandwidth of the link needed for a guard band of 10kHz frequency to prevent interference between six channels, each with 100kHz frequency is

A. 425kHz **B.** 575kHz

C. 650kHz **D.** 725kHz

28 If we correlate the received signal with any one of the two orthogonal function, the obtained inner product will be

A. In phase **B.** Quadrature

C. Zero **D.** Cannot be determined

29 In delta modulation, the slope overload distortion can be reduced by

A. Decreasing the step size **B.** Decreasing the granular noise

C. Decreasing the sampling rate **D.** Increasing the step size

30 The probability cumulative distribution function must be monotone and

A. increasing **B.** decreasing

C. Non decreasing **D.** Non increasing

PART B

(Answer all questions. Each question carries 2 marks)

31 The total gain of a multistage amplifier is less than the product of the gains of individual stages due to ……

A. Power loss in the coupling device **B.** Loading effect of the next stage

C. The use of many transistors **D.** The use of many capacitors

32 The two stages of a cascade amplifier have individual upper cut-off frequencies f1=5MHz and f2=3.33MHz. What is the best approximation for the upper cut-off frequency in cascade combination?

A. 4.16MHz **B.** 3.33MHz

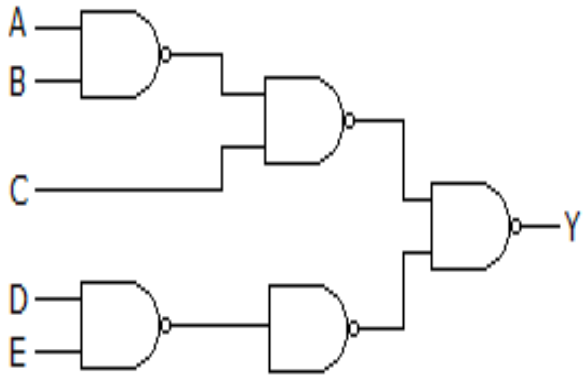
C. 2.5MHz **D.** 5MHz

33 A 4 bit ripple counter and a 4 bit synchronous counter are made using flip flops having a propagation delay of 10ns each. If the worst-case delay in the ripple counter and the synchronous counter be R and S respectively, then

A. R=10ns, S=40 ns **B.** R=40ns, S=10 ns

C. R=10ns, S=30 ns **D.** R=30ns, S=10 ns

34 The circuit of the given figure realizes the function .....



A. $Y = (\overline{A} + \overline{B})C + \overline{DE}$

B. $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}$

C. $AB + C + DE$

D. AB+C(D+E)

35 The frequency of oscillation of astable multivibrator with component values $R_1 = 2K\Omega$ $R_2 = 20K\Omega$ $C_1 = 0.01\mu F$, $C_2 = 0.05\mu F$ is

A. 1428.5 Hz **B.** 142.85 Hz

C. 14.285 Hz **D.** 1.4285 Hz

36 What is the maximum frequency for sine wave output voltage of 10v peak with an Op-amp whose slew rate is 1V/μs?

A. 15.92kHz **B.** 19.73kHz

C. 23.54kHz **D.** 27.336kHz

37 What is the folding frequency for the aliased version of x (n) with sampling rate F?

A. F/D **B.** F/4D

C. F/2 **D.** F/2D

38 The 4-point Discrete Fourier Transform (DFT) of a discrete time sequence {1,0,2.3} is

A. [0, -2+2j, 2, -2-2j] **B.** [2, 2+2j, 6, 2-2j]

C. [6, 1-3j, 2, 1+3j] **D.** [6, -1+3j, 0, -1-3j]

39 In Delta modulation_____

A. all the coded bits used for sampling are transmitted **B.** one bit per sample is transmitted

C. the step size is fixed **D.** Both A & B

40 A bandwidth of 10kHz is required for AM system. If the lowest frequency component in the modulated signal is 555kHz, carrier frequency in kHz is

A. 525 **B.** 550

C. 560 **D.** 565