Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SIXTH SEMESTER B.TECH DEGREE EXAMINATION (R), MAY 2023
ELECTRONICS AND COMMUNICATION ENGINEERING
(2020 SCHEME)

Course Code : 20ECT304

Course Name: VLSI Circuit Design

Max. Marks : 100 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. State Moore's law in VLSI design.
2. Give the advantages and disadvantages of cell-based ASIC design.
3. Draw the circuit diagram of NMOS and CMOS inverter.
4. Explain pass transistor logic with example.
5. Enumerate the merits of dynamic logic circuits.
6. Compare volatile and non-volatile memories.
7. Describe the need for high-speed adders. Give the applications of high-speed adders.
8. What is meant by data path?
9. Write a short note on electron beam lithography.
10. Explain the principle of molecular beam epitaxy with a schematic diagram.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) What is FPGA? What are its applications? With a block diagram explain its internal architecture? (8)
    b) Explain power consideration in ASIC (6)

OR

12. a) Explain ASIC Design Flow. (10)
    b) List the advantages of SOC. (4)

MODULE II

13. a) Realize an XOR gate using (9)
    i. CMOS logic ii. NMOS pass transistor logic iii. Transmission gate logic
    b) Explain about transient characteristics of CMOS. (5)

OR

14. a) Realize a NAND gate using CMOS logic and explain its operation. (7)
    b) Derive the expression for switching threshold of a CMOS inverter. (7)

MODULE III

15. a) Design a 4×4 ROM array using NAND and explain its working. (8)
    b) What is the "charge sharing" problem? Explain two methods with neat diagrams to overcome it. (6)

OR

16. a) Explain 'Precharge' and 'Evaluate' operations in dynamic logic circuits with the help of diagrams. (6)
    b) Explain the read and write operation of a three-transistor DRAM cell. (8)

MODULE IV

17. a) Explain the working of a 16-bit carry-bypass adder. (7)
    b) Show the critical path of an array multiplier. Estimate the delay. (7)

OR

18. a) Estimate the delay of an n bit linear carry select adder. (7)
    b) Illustrate the principle of operation of an array multiplier. (7)

MODULE V

19. a) Explain the fabrication steps of CMOS n-well process with the help of diagram. (8)
    b) Draw the stick diagram of CMOS inverter. (6)

OR

20. a) Explain the Ion implantation technique in IC fabrication with neat diagram. (7)
    b) Explain various layout design rules in CMOS fabrication with sample diagrams. (7)

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