Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FOURTH SEMESTER B.TECH DEGREE EXAMINATION (R), MAY 2023
ELECTRICAL AND ELECTRONICS ENGINEERING
(2020 SCHEME)

Course Code : 20EET206

Course Name: Digital Electronics

Max. Marks : 100 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Convert 192.86_{10} to binary and hexadecimal.
2. Explain the following terms with respect to logic family.
   a) Noise margin
   b) Fan out
   c) Propagation delay
3. State and explain the principle of duality and De-Morgan's theorem.
4. Obtain the truth table of the following function F1.
   F1=(A+B)(A'+B+C)(A+B'+C)
5. Illustrate the working of a parity encoder.
6. Explain the concept of arithmetic and logic unit.
7. Explain the differences between a characteristic table and an excitation table.
8. Differentiate edge triggered and level triggered flip flops.
9. How do you differentiate Mealy and Moore machines?
10. What do you mean by state transition diagram?

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Perform following operations on decimal numbers using 2's complement method. (i) 55-86 (ii) 68 –23 (8)
    b) Explain the following.
    (i) Excess-3 code(ii) Gray code (iii) ASCII code (iv) BCD code (iv) Parity codes (6)

OR

12. a) With the help of a suitable diagram, explain the working of a TTL NAND gate. (8)
    b) (i) Differentiate fixed point and floating-point representation.
    (ii) Represent $(1.27 \times 10^2)_{10}$ 10 fixed point and floating point Binary formats. (6)

MODULE II

13. a) Convert each of the following into the other canonical form
(i) $F(A, B, C) = \prod M(1,2,6)$ (ii) $F(A, B, C, D) = \prod M(1,3,5,8)$ (9)
(iii) $F(q, r, s, t) = \sum m(1,2,7,9,12)$
b) Simplify the Boolean function
$F(w, x, y, z) = \sum m(0,1,2,4,6,8,9, 13) + d(5,12,14)$ using K map and obtain simplified logic expression. (5)

OR

14. a) Explain the working of a carry look-ahead adder. What are the merits and demerits of it? (8)
b) Design a full subtractor and implement it using universal gates. (6)

MODULE III

15. a) Implement the logic function
$F(w, x, y, z) = \sum m(0,1,2,4,5,8,9,12,13,14)$ on an 8:1 multiplexer. (8)
b) Construct an 8:1 multiplexer using 4:1 multiplexers and explain its working. (6)

OR

16. a) Design and implement a 3-bit magnitude comparator. (9)
b) What is a priority encoder? Show the design of a 4-input priority encoder. (5)

MODULE IV

17. a) Design a Mod-7 synchronous up counter using JK flip flops. (10)
b) Construct a 4-bit shift register that performs SISO & PISO operations. (4)

OR

18. a) Design a sequential circuit that produces the following output sequence: 0000,1000,1100,1110,1111,0111,0011,0001,0000….. (7)
b) Design a Mod-6 asynchronous up counter with proper narration. (7)

MODULE V

19. a) Explain the construction and working of a Flash ADC. (8)
b) Write notes on PAL, PLA and FPGA. (6)

OR

20. a) With the help of suitable diagrams, illustrate the working of an R-2R ladder D/A converter. (8)
b) Write a VHDL program to describe a full adder. Show necessary diagrams (6)

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