Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FOURTH SEMESTER B.TECH DEGREE EXAMINATION (R), MAY 2023
COMPUTER SCIENCE AND ENGINEERING
(2020 SCHEME)

Course Code : 20CST202

Course Name: Computer Organization and Architecture

Max. Marks : 100 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Justify the need of memory addressing. What is the maximum amount of memory that can be addressed using a 32-bit address?
2. For small computer systems, what type of bus organization is needed: single bus or multiple bus? Give examples.
3. State the purpose of status register in processor and mention the common flags used in it.
4. Define inter-register transfer with an example.
5. Compare and contrast the instruction pipeline and arithmetic pipeline.
6. What is data hazard in pipelined processor? State what dependency arises in the following instructions:
   Mul R2,R3,R4
   Add R5,R4,R6
7. State the difference between horizontal and vertical microinstructions with suitable example.
8. Mention the steps to depict the control unit.
9. List the characteristics of semiconductor RAMs.
10. What are the hardware components involved in interrupt processing? State its functionality.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Explain instruction cycle in brief. Mention the steps involved to complete the DIV R1,R2 instruction. (8)
    b) Explain the usage of multiple bus organization in simple datapath for adding two numbers with its components. (6)

OR

12. a) Define addressing mode in detail and state its importance? With an example explain each addressing modes. (10)
    b) Discuss in detail about functional units of computer. (4)

MODULE II

13. a) Explain in brief about microperations and its types. Write a sequence of micro-operations to transfer data from register R1 to register R2 and multiply the contents of R3 to R2. Mention the inter-register transfers involved in each micro-operation. (10)
    b) What is logical shift-left, with an example comment the necessity of its usage? (4)

OR

14. a) Discuss the different types of ALU operations and their implementation in the processor. Design and implement 4-bit ALU which performs addition and subtraction. (10)
    b) Explain how data is stored and manipulated in the accumulator. With any example instruction brief the use of accumulator. (4)

MODULE III

15. a) Describe the restoring division algorithm for binary numbers along with its circuit arrangement. Perform restoring division for binary numbers with dividend 1000 and divisor 11 (10)
    b) How to handle data hazards and mention its side effects with an example. (4)

OR

16. a) Describe the Booth's multiplication algorithm, and explain how it can improve the efficiency when compared with traditional multiplication algorithm. Perform multiplication using booth's algorithm with M=23 and Q=-9 (10)
    b) Explain how pipelining can be used to speed up instruction execution in a processor with an example. (4)

MODULE IV

17. a) Describe the role and functions of microinstructions and microprogam sequencing in microprogrammed control unit with an example. (12)
    b) Mention the advantages and disadvantages of microprogrammed control unit. (2)

OR

18. a) Explain the implementation of control unit with hardwired implementation technique in detail. Consider any sequence of control signals for an instruction and design circuit for it. (12)
    b) What are the advantages and disadvantages of hardwired control and microprogrammed control unit approaches? (2)

MODULE V

19. Explain the concept of cache memory. Describe the different mapping techniques used to map memory blocks from main memory to cache. Discuss the advantages and disadvantages of each mapping technique with an example. (14)

OR

20. Describe in detail about direct memory access (DMA) and its applications. Illustrate the architecture of a DMA controller and how it interfaces with the CPU and I/O devices. Also, discuss the advantages and disadvantages of using DMA with an example. (14)

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