Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER M.TECH DEGREE EXAMINATION (Regular), MAY 2023

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: **21VE204-E**

Course Name: **Physical Design and Verification**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Describe inputs and outputs of synthesis in IC design.
2. Explain timing exceptions in IC design.
3. Enumerate the different steps in routing.
4. Explain floor planning in physical design and its inputs.
5. Explain why clock routing is done before signal routing.
6. List the various steps involved in analyzing a clock tree.
7. Explain cross clock balancing.
8. Explain timing analysis associated with physical verification

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

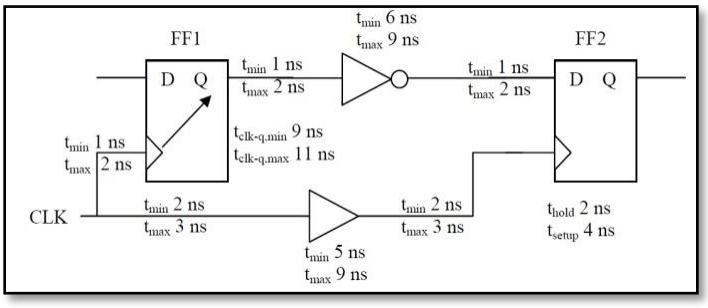
9. Summarize backend flow in IC design with an example. (6)

OR

10. Demonstrate the flow of synthesis with an example. (6)

MODULE II

11. Analyse the following circuit and calculate the maximum clock frequency that can be given to this circuit. (6)



OR

12. Consider a system with three flipflops fed with same clock of time period 10ns the latches are separated by two combinational paths (path 1 between FF1 and FF2, path 2 between FF2 and FF3). What will happen if the combinational logic delay is larger than 10ns, also what will happen if FF2 is replaced with a latch. (6)

MODULE III

13. Explain post route optimization and various issues in routing. (6)

OR

14. Describe various steps associated with LVS during physical design. (6)

MODULE IV

15. List the various steps associated with the floor planning in physical design. (6)

OR

16. Explain the use of blockages and congestion associated with floor planning. (6)

MODULE V

17. Illustrate any three CTS algorithm with neat sketches. (6)

OR

18. Explain useful clock skew with an example. (6)

MODULE VI

19. Explain various steps in physical verification of an IC design. (6)

OR

20. Show the significance of TCL scripting in physical design with any two example script. (6)

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