Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER M.TECH DEGREE EXAMINATION (Regular), MAY 2023

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: 21VE206-A

Course Name: High Speed Digital Design

Max. Marks: 60 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Determine the reactance of a high speed circuit with a capacitance of 150 pF and a resistance of 560 Ω at the rise times 1 ns, 3 ns and 12 ns.
2. In a decaying system, the value of the time constant at the (1-1/e) point of the rise time is 24 ns. Calculate the value of the decaying component if passes only very high frequency signals in the presence of a series resistance of 330Ω.
3. Illustrate using figures and summarize two methods by which cross talk may be observed when the system clock is slowed down at high frequencies.
4. Derive the characteristic equation of an ideal transmission line at high speeds.
5. Explain any two mechanical properties of vias.
6. Illustrate source termination and state any two characteristics of the same.
7. Examine clock skew at high speeds with the help of figures and equations.
8. Summarize the three power rules applicable to high speed circuits.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. Explain the speed of operation of a high speed digital circuits in terms of sudden changes in current.

   A TTL gate is loaded with a capacitive load of 22 pF. Assume the voltage swing is 4.8 V and the rise time is 1.85 ns. Find the rate of change of TTL output current. (6)

OR

10. Examine the relation of mutual inductance to cross talk.

    Determine the output resistance of a CMOS driver with the quoted (6)

ratings as given below at a power supply voltage of 4.8 V:

V_{OL} at I_O=3 mA
Typical value at 25^{0}C=0.12 V
Maximum value between -40^{0}C and 85^{0}C=0.4 V

V_{OH} at I_O=-3 mA
Typical value at 25^{0}C=4.5 V
Maximum value between -40^{0}C and 85^{0}C=3.5 V

MODULE II

11. Explain rise time and bandwidth of oscilloscope with necessary expressions and figures.

An oscilloscope rated at 310 MHz was purchased and its probe was also rated at 310 MHz. Both specifications are of RMS bandwidths. How will this combination affect the rise time of the signal displayed when the input signal has 2.1 ns rise time? (6)

OR

12. With the help of the electrical model of an oscilloscope, illustrate the estimation of self-inductance of probe ground loop, Q value and the effect of probe loading on a high speed circuit. (6)

MODULE III

13. Examine the problems of signal distortion in point-to-point wiring at high frequencies with necessary figures and equations. (6)

OR

14. 'Slowing down of a clock system affects the overall performance of a high speed digital system.' Explain the statement with special reference to meta-stability in clock distribution. (6)

MODULE IV

15. Explain Proximity effect and Dielectric loss associated with high speed digital circuits. (6)

OR

16. State the unique properties of lossless transmission lines. With the help of equations, diagrams and graphs, demonstrate that DC attenuation assumes greater values than travelling wave attenuation in lossy LRC transmission lines. (6)

MODULE V

17. Examine end terminations in the following respects (i) Rise time by intuition and calculation (ii) DC Biasing. (6)

OR

18. Illustrate the capacitance associated with connectors. (6)

MODULE VI

19. Elaborate on the design of the set of bypass capacitors used for the uniform distribution of a stable reference voltage in a high frequency digital system. (6)

OR

20. Explain delay adjustments at high frequencies and elaborate on the different types of delays using apt illustrations. (6)

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