Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER M.TECH DEGREE EXAMINATION (Regular), MAY 2023

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: 21VE205-C

Course Name: Computer Architecture and Parallel Processing

Max. Marks: 60 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Explain multithreading and its various implementations.
2. Write the processor performance equation and define the terms.
3. Explain the concept of speculative execution in dynamic scheduling.
4. Define Hit time, Miss Penalty and Average memory access time.
5. With a suitable diagram, explain about computer memory hierarchy.
6. Discuss in brief on the different distributed memory architectures.
7. Describe the SMT multithreaded architecture with suitable diagram.
8. Differentiate between software and hardware multithreading.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. Describe the dataflow architecture with a sample dataflow machine. (6)

OR

10. Explain the different classes of shared memory multiprocessors with suitable block diagrams. (6)

MODULE II

11. Differentiate RISC and CISC ISA architectures with suitable example. (6)

OR

12. What are hazards and describe various pipeline hazards? (6)

MODULE III

13. Describe the compiler optimization techniques for exploiting ILP? (6)

OR

14. What are name dependencies between instructions and how they can be eliminated? (6)

MODULE IV

15. Illustrate any two mapping methods in cache memory with suitable diagrams. (6)

OR

16. Explain with a neat diagram how virtual memory address is translated to physical address. (6)

MODULE V

17. An L1 cache memory has an access time of 12ns and miss rate 6%. An optimization was made to reduce the miss rate to 4% but the hit latency was increased to 16ns. Under what circumstance, this optimization would result in a performance improvement. (6)

OR

18. A cache has hit rate of 90%, block size of 128 bytes, cache hit latency of 5ns. Main memory takes 50ns to return first word (32 bits) of a block and 10ns for each subsequent word. Calculate the miss latency of the cache and if the cache block size is doubled which eventually reduced the miss rate to 3%, does it reduce AMAT? (6)

MODULE VI

19. Explain about the models of memory consistency. (6)

OR

20. Explain Buses and Crossbar switch interconnection networks for parallel systems. (6)

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