Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER M.TECH DEGREE EXAMINATION (Regular), MAY 2023

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: 21VE202

Course Name: Advanced CMOS VLSI Design

Max. Marks: 60 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Why low power has become an important issue in the present-day VLSI circuit realization.
2. List various sources of power dissipation in CMOS Circuits.
3. Give the advantages and limitations of MTCMOS approach
4. List the salient features of domino logic family.
5. Realize XOR/XNOR gates using DCVS
6. Describe adiabatic logic circuit.
7. What are the major sources of power wastage in SRAM.
8. What are the advantages of the banked organization?

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. Describe with the aid of diagrams and equations, how velocity saturation, which is one of the problems caused by short channel effect affect the performance of a submicron channel device. (6)

OR

10. Explain Drain Induced Barrier Lowering (DIBL) in MOSFET devices. How it leads to punch through. (6)

MODULE II

11. Illustrate short circuit power dissipation. (6)

OR

12. Derive an expression for dynamic power dissipation. How it can be reduced? (6)

MODULE III

13. Explain various leakage mechanisms in deep submicron transistors. (6)

OR

14. Analyze a conventional two input CMOS NAND gate circuit. Explain how Stacking effect can be used in stand by leakage current reduction. (6)

MODULE IV

15. List the salient features of dynamic logic. Realize ab + (c+d) (e+f) + gh using domino logic. (6)

OR

16. Explain the race problem in dynamic logic addressed in the NORA CMOS circuit. (6)

MODULE V

17. Implement the function Z = (X1+X2) (X3 + X4) +X5 X6 using dynamic logic. (6)

OR

18. Show how the function AB+BC+CA can be realized using a DCVS logic using suitable diagrams. (6)

MODULE VI

19. Sketch the schematic diagram of a SRAM memory cell along with sense amplifier. Explain how read operations is performed. (6)

OR

20. Describe various low-voltage low-power SRAM cell designs. Explain any two. (6)

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