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# SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

**FIFTH SEMESTER B.TECH DEGREE EXAMINATION (Regular), DECEMBER 2022**

**(2020 SCHEME)**

**Course Code : 20ECT391**

**Course Name: FPGA Based System Design**

**Max. Marks : 100** **Duration: 3 Hours**

## PART A

***(Answer all questions. Each question carries 3 marks)***

1. Write down the difference between Field Programmable Gate Arrays and Application Specific Integrated Circuits.
2. Describe the coding style of VHDL with example.
3. Distinguish between FPGA and CPLD.
4. Enlist the difference between PAL and PLA using logic diagrams.
5. Describe Look Up Table (LUT) with an example.
6. Describe the Xilinx/Altera vendor issues in logic block architecture of FPGA.
7. List the type of partitioning in FPGA.
8. Sketch the FPGA design workflow diagram.
9. List any six commercially available FPGAs.
10. Sketch the general architecture of Altera FPGA.

## PART B

***(Answer one full question from each module, each question carries 14 marks)***

### MODULE I

11. a) Define the term state machine. With the aid of suitable logic diagram describe the importance of state machines in digital system design. (7)

    b) Write a verilog module and test bench for a positive edge triggered flip-flop using behavioral modeling (7)

**OR**

12. Consider an example of one-bit full adder, explain the behavioral specification of hardware and give its behavioral description using Verilog with a test bench. (14)

### MODULE II

13. Sketch and explain the programming technologies in FPGA. (14)

**OR**

14. Implement the given min boolean function using 3 × 4 × 2 PLA. A1 (A, B, C) = (0, 1, 3, 4) and A2 (A, B, C) = (1, 2, 3, 4, 5). (14)

**MODULE III**

15. Sketch and explain the different programmable elements in FPGA architecture. (14)

**OR**

16. Compare coarse- and fine-grained FPGA architecture with diagrams. (14)

**MODULE IV**

17. Explain partitioning and placement processes in FPGA. (14)

**OR**

18. Explain embedded system design using FPGAs. (14)

**MODULE V**

19. Sketch and explain the architecture of Xilinx XC4000 FPGA. (14)

**OR**

20. Explain the architecture of Actel (Act-1 & Act-2) FPGAs. (14)

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