G 1466

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Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2016

Sixth Semester

Branch : Applied Electronics and Instrumentation Engineering

AI 010 606 L 03—DIGITAL SYSTEM DESIGN (Elective I) (AI)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours

Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. Differentiate between FPGA and CPLD.
2. List the applications of RS485.
3. Draw a general model of Moore machine.
4. State the rules for writing an identifier.
5. List the basic steps for the synthesis of a sequential circuit.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Give the important characteristic features of XILINX FPGA.
7. List out the standard specifications of RS232.
8. Draw the state diagram, state table and ASM chart for a JK flip-flop.
9. How is a "package" defined in a VHDL program ? Give an example.
10. Explain the steps, how to design a synchronous circuit.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Derive PLA implementation of a full adder and explain.

Or

12. Draw and explain the architecture of a ROM. How it can be used to implement as a memory, and as to realise a logic expression.

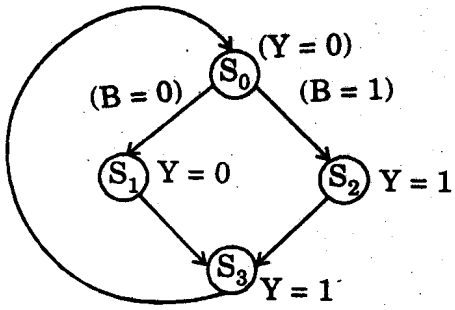
Turn over

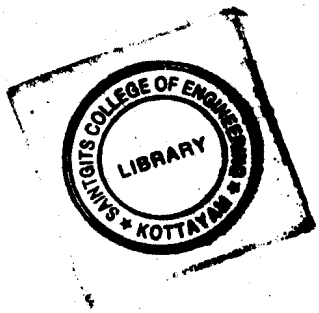
13. Explain the functions and uses of IIC bus. How it is interfaced with a processor ?

Or

14. Explain the functions of the control and data signals in a typical bus interplace IC.

15.





The state diagram for a sequential circuit is given above. Derive the (i) next state table ; (ii) implementation table using D flip-flops and (iii) final FSM circuit.

Or

16. Explain how a BCD to excess-3 code converter can be realized as Mealy sequential machine. Draw the state diagram and state table for the same.

17. (a) List the various sequential statements used in VHDL. Explain any *two*. (6 marks)

(b) Write the VHDL code for 3-to-8 decoder with enable input and active high output. (6 marks)

Or

18. (a) Explain the access data type with an example. (3 marks)

(b) Give the structural VHDL code to model 4-bit carry ripple adder. Use generate statement. (9 marks)

19. (a) Write the behavioural code for T flip-flop with synchrous reset and preset. Explain. (6 marks)

(b) Write the behavioural code for the BCD up-down counter. (6 marks)

Or

20. Write the structural VHDL code for the binary up-down counter with parallel load to construct an up-down counter circuit that outputs the sequence :

4, 8, 5, 3, 16 and 7 repeatedly.

(5 × 12 = 60 marks)