F 3190 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Fifth Semester

Branch : Electronics and Communication/Applied Electronics and Instrumentation Engineering

COMPUTER ORGANISATION AND ARCHITECTURE (LA)

(Old Scheme—Supplementary/Mercy Chance)

[Prior to 2010 Admissions]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 4 *marks.*

1. Explain index addressing with an example.
2. Write a note on floating point number representation.
3. Draw and explain a typical hardwired control unit.
4. What do you mean by instruction execution cycle ?
5. What is a hard disk ? Name three different types of hard disks. Write a typical usage of each type.
6. What is a cache memory ? How it is different from a primary memory ?
7. What is a plotter ? What types of users need it ?
8. What is bus arbitration ? Explain its classification.
9. How is multiprocessing different from multiprogramming ?
10. What is multitasking ? What are the similarities and differences between Multitasking and Multiprocessing ?

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. (a) What is an addressing mode ? Explain different types of addressing modes. (6 marks)

    (b) Explain fast adder. Write the number of gate delays required to perform n-bit addition using ripple carry adder and fast adder.

    (6 marks)

Or

12. What is Booth's algorithm ? Explain. Multiply 23 × – 5 using Booth's algorithm.

Turn over

13. (a) With a neat diagram, which shows the separation of decoding and encoding functions, explain the hardwired control. (6 marks)

(b) Show the microinstruction sequencing with next address field. (6 marks)

Or

14. (a) Explain the concept of microprogrammed control. (6 marks)

(b) Show the control sequences for execution of ADD (R3) R1 and explain. (6 marks)

15. (a) Compare and distinguish between logical address and physical address. (6 marks)

(b) Explain how the translation buffers speed up logical address generation. (6 marks)

Or

16. (a) With neat diagrams, explain the operation of a 1M × 1 dynamic memory and its working. (6 marks)

(b) What is the need of cache replacement algorithms ? Explain LRU replacement algorithm. (6 marks)

17. What is DMA ? How it is different from programmed I/O and interrupt driven I/O ? Explain with suitable examples.

Or

18. (a) Why bus arbitration is required ? Explain with block diagram bus arbitration process using daizy chain arrangement. (7 marks)

(b) Explain the steps involved in handling interrupt. (5 marks)

19. (a) What is a Cache coherence ? Explain any *one* cache coherence protocol used in multiprocessor system. (6 marks)

(b) Explain the architecture of an array processor. (6 marks)

Or

20. What is multiprocessing ? Draw basic organisation diagram of a typical multiprocessing system and explain its features. Distinguish between tightly coupled and loosely coupled multiprocessing system.

[5 × 12 = 60 marks]