Register No.:   ………………………………   Name: …………………………………………………………

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER B.TECH DEGREE EXAMINATION (Regular), DECEMBER 2022
COMPUTER SCIENCE AND ENGINEERING
(2020 SCHEME)

Course Code: **20CST203**

Course Name: **Logic System Design**

Max. Marks: **100**   **Duration: 3 Hours**

PART A
(Answer all questions. Each question carries 3 marks)

1. Find the value of **b** ? given that $16_{10} = 100_b$
2. Write short notes on ASCII, EBCDIC with suitable example?
3. State and Prove De Morgan's Theorem?
4. Show that $A\overline{B}C + B + \overline{A}C + AB\overline{D} + B\overline{D} = B+C$
5. Realize a 2-bit magnitude comparator.
6. What are the differences between serial and parallel adders?
7. Construct D flip-flop using NAND gates. Also give its excitation Table.
8. What is the difference between a latch and a flip-flops.
9. What is ROM ? Explain with Diagram.
10. What is the basic architecture of Programmable Logic Array?

PART B
(Answer one full question from each module, each question carries 14marks)

MODULE I

11. a) Perform the following operations in 8421 BCD code(i) 679.6 + 536.8 (ii) 206.7 - 147.8 , Show the steps clearly   (8)
    b) Divide 32 by 5 in binary using the computer method.   (6)

OR

12. a) Perform the following operations (i) $25_8 - 73_8$ (ii) $3A_{16} - 5D_{16}$ (8)
    b) Find the 16 bit 2's complement representation of the following Binary numbers. (i) +1001010 (ii) – 11110000 (iii) – 11001100.1   (6)

MODULE II

13. a) Realize a XNOR circuit using NAND gate only.   (5)
    b) Minimize in SOP and POS forms on the K-Map the 5-Variable function.
       F = $\Sigma m(0,1,4,5,6,13,14,15,22,24,25,28,29,30,31)$ (9)

OR

14. a) Using K-map, simplify the Boolean Function F in SOP form, using the don't care conditions d: F(w, x, y,z) = w′(x′y + x′y′ + x yz) + x′z′(y + w) d(w, x, y,z) = w′x(y′z + yz′) + w yz.   (8)

    b) Expand A($\overline{B}$ + A)B to maxterms and minterms.   (6)

MODULE III

15. a) Implement a Full Adder circuit using 4:1 MUX.   (8)

    b) With a neat diagram explain 4-bit carry look-ahead adder.   (6)

OR

16. a) Design and implement a code converter for converting 4-bit Gray to Binary code.   (10)

    b) Implement Half Subtractor circuit using NOR gate only.   (4)

MODULE IV

17. a) Set up an asynchronous Counter that count the sequence 1,3,5,7 with minimum number of flip-flops.   (5)

    b) Design a synchronous 3-bit Binary Up-Down Counter using JK-FF.   (9)

OR

18. a) Write short notes on Master Slave JK flip-flop ?   (4)

    b) Design a counter that count the states 3,4,6,7 and 3... using JK flip- flops.Is the counter is self-starting ?   (10)

MODULE V

19. a) Draw the logic diagram of a 4-bit bidirectional serial in serial out (SISO) shift register with mode control and explain the working with timing diagram.   (9)

    b) Write an algorithm for floating point subtraction.   (5)

OR

20. a) Draw the logic diagram of a 4-bit Johnson counter and explain the working with truth table and Timing diagram.   (8)

    b) Implement 3-bit binary to gray conversion using Programmable Logic Array.   (6)

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