Register No.: .... Name: ....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER B.TECH DEGREE EXAMINATION (Regular), DECEMBER 2022
ELECTRONICS AND COMMUNICATION ENGINEERING
(2020 SCHEME)

Course Code :   **20ECT203**

Course Name: **Logic Circuit Design**

Max. Marks :   **100**   **Duration: 3 Hours**

PART A
(Answer all questions. Each question carries 3 marks)

1. (i) Convert $(110101.101010)_2$ to octal and hexadecimal.
   (ii) Represent 478_{10} in BCD and Excess-3 code.

2. Represent $(-51)_{10}$ in (i) Sign magnitude (ii) 1's complement form (iii) 2's complement form.

3. State and prove De-Morgan's Theorem.

4. Explain the different types of operators in Verilog.

5. Design a 3:8 decoder with diagram.

6. What is race around condition and how it is eliminated?

7. Write the characteristic table and excitation table of SR Flip flop.

8. Define the following (i) Fan - in (ii) Fan-out

9. Write the program for 2-bit asynchronous UP counter using gate level modelling.

10. Implement verilog code for JK Flip flop.

PART B
(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Explain the floating point and fixed-point representation of numbers.   (8)

    b) Generate Hamming code for the message 1110 in EVEN parity and ODD parity.   (6)

OR

12. a) Explain Verilog HDL data types with example.   (8)

    b) Perform the following operation using 2's complement method.
   a) $(1111)_2 - (1010)_2$ b) $(1000)_2 - (1010)_2$ (6)

MODULE II

13. a) Reduce the expressions   (i) AB+A(B+C)+B(B+C),   (8)

                           (ii) [A'[B+C(A'B+AC)]]'

   b) Write Verilog program for XOR using NOR in Gate level modelling   (6)

OR

14. a) Realize the logic function using basic logic gates   (8)
   F(A,B,C,D) = Σm(0,1,2,5,6,8) + d(3,4,7,14)   using K-map
   b) Write Verilog program for XOR using NAND in Gate level modelling   (6)

MODULE III

15. a) Design and implement a 4:1 Multiplexer.   (6)
   b) Illustrate the working of a BCD adder.

                                                                (8)

OR

16. a) Design and implement a 2-bit comparator.   (7)
   b) Write down the Verilog code for full adder using gate level modelling.   (7)

MODULE IV

17. a) Convert **SR** Flip flop to **JK** Flip flop and **T** Flip flop.   (6)
   b) Design and explain a MOD 8 asynchronous down counter.

                                                                (8)

OR

18. a) Design and explain 4-bit Ring counter with necessary diagrams.   (6)
   b) Design a 3-bit synchronous UP counter using JK FFs.   (8)

MODULE V

19. a) Explain different electrical characteristics of logic gates.   (6)
   b) Illustrate the operation of TTL Inverter.   (8)

OR

20. a) Draw the circuit of a CMOS inverter and explain its operation.   (6)
   b) Illustrate the operation of TTL NAND.   (8)

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