Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FIRST SEMESTER M.TECH DEGREE EXAMINATION (Regular), DECEMBER 2022

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: 21VE104-E

Course Name: ASIC Design and Verification

Max. Marks: 60 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Describe the program structure of Verilog with an example.
2. List out two low-power techniques employed in modeling of circuits using Verilog.
3. List out major data types in system verilog with an example.
4. Describe SV assertions in system verilog.
5. Illustrate the significance of factory registration in UVM based test bench.
6. List out three UVM components.
7. Describe 'configurations' in UVM.
8. Illustrate Register abstraction layer in UVM.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. Design a 4-bit generic ALU in Verilog. (6)

OR

10. Design a 4-bit up/down counter in Verilog. (6)

MODULE II

11. List the various steps involved in Finite State Machine modelling in Verilog with an example. (6)

OR

12. Illustrate a 4×1 multiplexer using structural modelling and its testbench. (6)

MODULE III

13. Explain System Verilog Mailbox with a generic example. (6)

OR

14. Differentiate Queue and Stack in System Verilog. (6)

MODULE IV

15. Interpret Code Coverage and functional coverage in System Verilog. (6)

OR

16. Demonstrate memory test bench using System Verilog. (6)

MODULE V

17. Summarize the role of RAL in verification scenario. (6)

OR

18. Describe the sequence of common phases that are executed in UVM. (6)

MODULE VI

19. Illustrate UVM RAL model with its advantages. (6)

OR

20. Discuss APB memory test bench using UVM. (6)

****