Register No.: .... Name: ....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FIRST SEMESTER M.TECH DEGREE EXAMINATION (Regular), DECEMBER 2022

VLSI AND EMBEDDED SYSTEMS

(2021 Scheme)

Course Code: **21VE102**

Course Name: **Advanced Digital Design**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Design and sketch a 110 sequence detector using Moore machine.
2. Sketch the logic circuit for the following Boolean function. F= AB'+BC. Analyze the possibility of Static 1 hazard in the circuit.
3. Sketch the circuit of a 3-bit parallel load shift right register and explain.
4. Draw the high-level state diagram for a Soda Dispensing system processor.
5. Define clock skew and jitter.
6. Describe any two methods for avoiding clock skew.
7. Explain the approach for automated two-level logic size optimization.
8. Define state encoding.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9.	Draw the Mealy State Diagram and State Table of sequence detector to detect input sequences 0110.	(6)

OR

10.	Design and draw the circuit for modulo 5 counter and write down the Verilog HDL code for it.	(6)

MODULE II

11.	Explain static hazards with an example.	(6)

OR

12.	Differentiate critical race and non-critical race.	(6)

MODULE III

13.	Design and sketch a 4 bit carry-ripple adder and explain.	(6)

OR

14. Design a 4-bit equality comparator and sketch the circuit diagram. (6)

MODULE IV

15. Explain the standard controller architecture for implementing an FSM as a sequential circuit. (6)

OR

16. Describe significance of Micro-programmed control unit in microprocessor design. Explain few control signal generations. (6)

MODULE V

17. Explain the general method for RTL design. (6)

OR

18. Design a processor for a soda dispenser and sketch the circuit. (6)

MODULE VI

19. For the following functions, find all of the prime implicants using the Quine-McCluskey method. (6)
 $f(a, b, c, d) = \Sigma\, m(0\ 3\ 5\ 7\ 8\ 14\ 13)$, Realize the optimized logic circuit.

OR

20. Explain carry-lookahead adder. (6)

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