G 548 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Fourth Semester

Branch : Electronics and Communication/Applied Electronics and Instrumentation/Electronics and Instrumentation Engineering

DIGITAL ELECTRONICS AND LOGIC DESIGN (LAS)

(Old Scheme—Supplementary/Mercy Chance)

[Prior to 2010 admissions]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 *marks.*

1. What are De Morgan's theorems ? Write them in equation form. Prepare their truth tables to prove their correctness.
2. What is meant by open collector output of TTL gate ? What is its utility ? Explain.
3. What are minterms and maxterms ? Give examples for which form of expressions do they occur.
4. Explain the essential features of K-map. What are their advantages and disadvantages ?
5. Implement a half adder circuit using NOR gates only.
6. Define and distinguish between half subtractor and full subtractor.
7. What are the differences between the operation of edge triggered flip-flop and master slave flip-flop ?
8. What are the differences between truth table and excitation table ? Give examples.
9. What are the differences between serial and parallel transfer ? Explain.
10. Draw the basic circuit of a ROM cell and explain its working.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. (a) What is the principle of operation of Schottky TTL ? Explain with a neat circuit diagram, the operation of a Schottky TTL.

(8 marks)

(b) Implement XOR using NOR gates only. Draw the circuit diagram. (4 mark)

Or

Turn over

12. (a) With circuit examples, show that a positive logic OR gate and a negative logic AND gate or vice versa are the same. (6 marks)

(b) Obtain a NAND gate realization of the Boolean expression :

$$f\ (A, B, C) = \left(A + \bar{B} + C\right)\left(\bar{A} + \bar{B} + \bar{C}\right)\left(\bar{A} + B\right).$$

(6 marks)

13. (a) Find the minimal sum and minimal product for th following functions using K-map :

$f_1 = \Sigma m\ (1, 3, 4, 5, 6, 7)$

$f_2 = \Sigma m\ (2, 3, 4, 5, 7)$.

(3 + 3 = 6 marks)

(b) Implement the Boolean function $f(w, x, y, z) = \Sigma m\ (0, 1, 5, 6, 7, 9, 12, 15)$ using 8 to 1 multiplexer. (6 marks)

Or

14. (a) Implement a full adder circuit using a decoder and two OR gates. (6 marks)

(b) Obtain the NOR gate realisation of the Boolean expressions :

(i) $f_1\ (w, x, y, z) = \Sigma m\ (0, 3, 6, 9, 10, 12, 15)$. (3 marks)

(ii) $f_2(a, b, c, d) = \bar{a}\,\bar{c}\,d + \bar{a}cd + \bar{b}\,\bar{c}\,\bar{d} + a\bar{b}\bar{c}$. (3 marks)

15. Draw the truth table of full subtractor. Using K-maps, design the minimal logic circuit using only NAND gates.

Or

16. Design a circuit for 4-bit 2's complement adder and realise it using only basic logic gates.

17. Draw the circuit diagram of a D flip-flop using only NAND gates and explain with the help of its truth table and excitation table.

Or

18. Draw the circuit diagram of clocked SR flip-flop constructed using fundamental logic gates. Explain its working with the help of timing diagrams. What are its demerits and how they are overcome ?

19. Design a synchronous mod-6 counter using clocked JK flip-flops with the help of excitation tables and K-maps. Draw the minimal circuit diagram and the timing diagram.

Or

20. Draw the organisation of a programmable ROM circuit. Explain the read and write operations clearly.

[5 × 12 = 60 marks]