Register No.: …… Name: ……..

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FOURTH SEMESTER B.TECH DEGREE EXAMINATION (S), SEPT 2022
ELECTRICAL AND ELECTRONICS ENGINEERING
(2020 SCHEME)

Course Code : **20EET206**

Course Name: **Digital Electronics**

Max. Marks : **100** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Convert the given decimal numbers to binary (i) 81.25 (ii) 99.75 (iii) 102.125
2. Which are the different types of parity codes used in modern digital systems?
3. Prove the second law of De Morgan's theorem.
4. Convert the function Y = A'B + ABC to standard Sum of Products expression.
5. Implement a 4:1 multiplexer using a 2:1 multiplexer.
6. Draw the diagram of a 2-bit magnitude comparator.
7. If NOT gates, AND gates and JK flip flop ICs are available, how will you convert an UP counter to a DOWN counter?
8. State the differences between synchronous and asynchronous counters.
9. What are the differences between Moore and Mealy machines?
10. Justify that successive approximation ADC is the fastest ADC.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Write notes on any three number systems in digital electronics. (9)
    b) Draw the internal diagram of a TTL NAND gate with totem pole output. (5)

OR

12. a) Implement a two input EX-OR gate using NAND gates. (9)
    b) Draw the internal diagram of a CMOS NOR gate. (5)

MODULE II

13. a) Using K-Map, find the minimal POS expression if Y = ABC + A'B'C + A'B'C' + A'BC (10)
    b) What is the difference between a full adder and a half adder? (4)

OR

14. a) Using K-Map, find the minimal SOP expression if Y = (A + B) (A'+B+C) (A'+B'+C') (A'+C) (11)
    b) How will you convert an adder to a subtractor? (3)

MODULE III

15. Design a BCD to Seven segment decoder. (14)

OR

16. a) Implement the function Y = ABC + A'B'C' + AB'C + A'BC using 8:1 multiplexer (7)
    b) Implement a 1:8 de-multiplexer using 1:4 de-multiplexers. (7)

MODULE IV

17. Design a 4-bit synchronous counter using MS JK flip-flops. (14)

OR

18. With neat diagram, explain the operation of a MOD10 asynchronous counter using MS JK flip-flops. (14)

MODULE V

19. a) With neat diagrams, explain the working of a flash ADC. (10)
    b) Write short notes on PLA and PAL. (4)

OR

20. a) Design a 4-bit weighted resistor DAC with a resolution of 0.5 V. (12)
    b) Write VHDL code for an AND gate. (2)

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