Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FOURTH SEMESTERB.TECH DEGREE EXAMINATION (Regular), JULY 2022
ELECTRICAL AND ELECTRONICS ENGINEERING
(2020 SCHEME)

Course Code: **20EET206**

Course Name: **Digital Electronics**

Max. Marks: **100** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Write the binary, octal and hexadecimal equivalents of 364.25
2. Write briefly about floating-point representation of binary numbers
3. What do you mean by standard form of a Boolean expression?
4. Draw the diagram of a 4-bit adder-subtractor?
5. What is the importance of a parity generator?
6. What is the difference between an encoder and a decoder?
7. Explain the excitation table of a JK flip-flop?
8. Draw the diagram of an asynchronous Mod 10 counter?
9. What are the limitations of a binary weighted resistor DAC?
10. Write the VHDL code for a half adder circuit?

PART B

(Answer one full question from each module, each question carries 14marks)

MODULE I

11. a) What is an excess-3 code? Explain with examples and mention its applications. (7)
    b) With necessary examples, explain the addition of two 4-bit numbers. (7)

OR

12. a) Justify the term "Universal Logic Gates" with suitable example. (8)
    b) Draw and explain the internal diagram of two input TTL NAND gate. (6)

MODULE II

13. a) Minimize the expression Y = ABC + A'B'C' + AB'C + A'B'C using K map (10)
    b) Explain the truth table of a half subtractor? (4)

OR

14. a) Minimize the expression Y = (A+B+C) (A'+B+C) (A'+B'+C) using K map (10)
    b) What are the advantages of a Carry Look Ahead adder? (4)

MODULE III

15. a) Implement a 4-bit magnitude comparator using two 2-bit magnitude comparators. (8)
    b) Explain an encoder with suitable example. (6)

OR

16. a) Realize the function Z = (A+B+C).(A+B+C').(A'+B+C).(A'+B+C) using 4:1 multiplexer (9)
    b) Realize a 1:8 demultiplexer using 1:4 demultiplexers. (5)

MODULE IV

17. a) What are the different types of shift registers? (6)
    b) Design a 3-bit asynchronous up counter. (8)

OR

18. Design a 3-bit synchronous up/down counter using JK Flipflops. (14)

MODULE V

19. a) What is a state machine? Explain different types of state machines. (9)
    b) Using a PLA, realize the function ABC + A'BC + ABC' + A'B'C'. (5)

OR

20. a) What is a FPGA? What are the advantages of using a FPGA? (9)
    b) What is VHDL? Explain structure of a VHDL program. (5)

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