Register No.: …… Name: ……..

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER M.TECH DEGREE EXAMINATION (Regular), JULY 2022

COMPUTER SCIENCE AND SYSTEMS ENGINEERING

(2021 Scheme)

Course Code: **21SE201**

Course Name: **Computer System Design and Architecture**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Differentiate between implicit parallelism and explicit parallelism.
2. Discuss various hazards in Pipelining.
3. List and explain different classification of vector processors.
4. Justify the statement "A good cache designer always prefers to have fully associative mapping rather than a direct mapping".
5. What is mirroring? What are its advantages and disadvantages?
6. A system uses 3 page frames for storing process pages in main memory. It uses the Least Recently Used (**LRU**) page replacement policy. Assume that all the page frames are initially empty.
   What will be the total number of page faults that might occur while processing the page reference string given below?
   4, 7, 6, 1, 7, 6, 1, 2, 7, 2
7. Define software and hardware multithreading.
8. What are the advantages that a designer can guarantee by using a distributed shared memory?

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. With neat sketch explain the different Flynn's taxonomies of computer architecture? (6)

OR

10. Illustrate the following architectural models and briefly explain
    a). UMA multiprocessor model (6)
    b). COMA multiprocessor model

MODULE II

11. With a neat diagram explain Tomasulo algorithm for out of order execution? (6)

OR

12. a) List out the situations where Pipelining architecture can be recommended. (3)
    b) An instruction pipeline consists of 4 stages:

    Fetch(F), Decode operand field (D), Execute (E), and Result-Write (W). The five instructions in a certain instruction sequence need these stages for the different number of clock cycles as shown by the table below.

Instruction	F	D	E	W
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1
5	1	2	1	2

(3)

    Find the number of clock cycles needed to perform the 5 instructions.

MODULE III

13. With a neat sketch explain memory hierarchy design. (6)

OR

14. With a neat sketch explain the working of GPU. What are its advantages to that of a normal processing unit? (6)

MODULE IV

15. A cache designer like to increase the performance of a cache by reducing the miss rate, as an expert in this area suggest the designer some ideas to achieve the goal. (6)

OR

16. a) Discuss the parameters used for measuring cache performance. (3)
    b) Assume that for a certain processor, a read request takes 50ns on a cache miss and 5ns on a cache hit. Suppose while running a program, it was observed that 80% of processor's read requests result in cache miss. Find the average access time in nanoseconds. (3)

MODULE V

17. Draw a neat sketch for the following RAID (6)
    a) RAID 0+1 b) RAID 1+0

OR

18. Define the following terms: (6)
    a) Multi programming b) Time sharing c)Multi processor systems

MODULE VI

19. With neat sketch explain Distributed Shared Memory and Centralized Shared Memory system with advantages and disadvantages. (6)

OR

20. What is multi-threading? Explain Software and Hardware multi-threading. (6)

****