Register No.: …… Name: ……..

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER B.TECH DEGREE EXAMINATION (S), MAY2022

ROBOTICS AND AUTOMATION

(2020 SCHEME)

Course Code: **20RBT203**

Course Name: **Electronic Devices and Circuits**

Max. Marks: **100** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Design a circuit which is used to remove the positive cycle of the input
2. What is the function of emitter bypass capacitor in CE amplifier?
3. A JFET has a drain current of 15 mA. If I_{DSS} is 25 mA and V_P is 5 V. Calculate V_{GS}
4. Explain gain bandwidth product of an amplifier?
5. What is cross over distortion? How it is eliminated?
6. An amplifier has a mid-frequency gain of 100 and a bandwidth of 200 KHz. What will be the new bandwidth and gain if 5% negative feed back in introduced?
7. Define CMRR
8. List the characteristics of an ideal Operational amplifier
9. Explain the function of voltage control oscillator in a PLL.
10. What is the significance of slew rate?

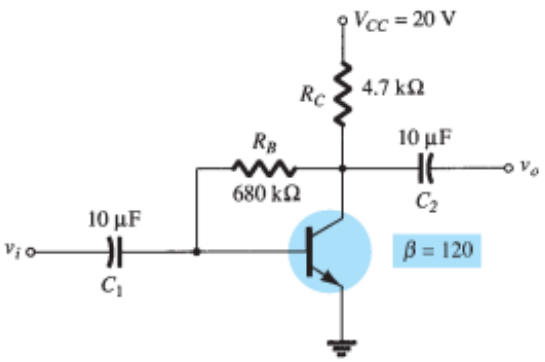
PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

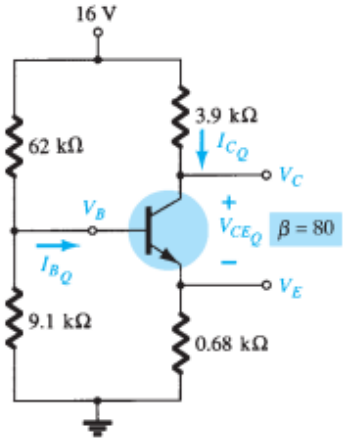
11. a) Explain the working of positive clamper circuit with neat diagrams. (7)

    b) For the given bias network determine the operating point. (7)



OR

12. a) For the given voltage divider biasing network determine the operating point. (6)



b) Using h parameter model derive voltage gain, current gain, input impedance, output impedance of a common emitter amplifier circuit. (8)

MODULE II

13. a) Explain the working of N channel JFET with suitable diagrams. (7)

b) What is Miller's theorem? Explain and prove it. (7)

OR

14. a) Analyze common source amplifier using small signal equivalent model. (7)

b) Determine the overall upper cut-off frequency of common emitter amplifier. (7)

MODULE III

15. a) Explain the working of Transformer Coupling scheme with its advantages. (9)

b) Prove that negative feedback improves gain stability. (5)

OR

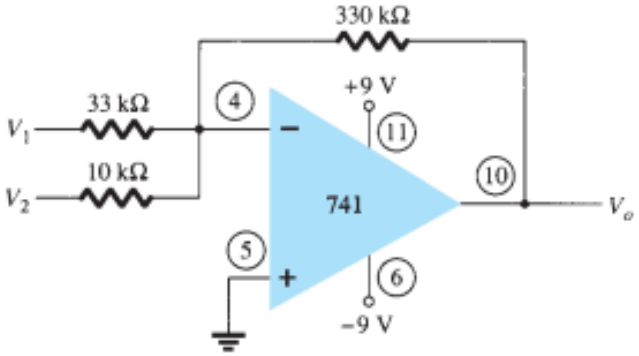
16. a) Identify a feedback topology which increases input and output impedances due to feed back. Prove the same (8)

b) Explain the working of class B power amplifier circuit. (6)

MODULE IV

17. a) Derive the frequency of oscillation of BJT RC phase shift oscillator. (9)

b) Calculate the output voltage for the circuit below for the inputs V_1= 50 mV sin(1000t) and V_2=10 mV sin(3000t). (5)



OR

18. a) Explain the working of Hartley oscillator. (8)

b) Realize a circuit to obtain $V_{out}=-5V_1+3V_2+4V_3$ using an operational amplifier. Use the minimum value of resistance as 10kΩ. (6)

MODULE V

19. a) Explain the operation of PLL with neat block diagram. (5)

b) With necessary diagrams, explain the working of astable multivibrator using 555 timer IC. (9)

OR

20. a) Explain the working of (i) integrator circuit (ii) triangular wave generator using operational amplifier. (10)

b) A dc voltage supply provides 60 V when the output is unloaded. When connected to a load, the output drops to 56 V. Calculate the value of voltage regulation. (4)

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