Register No.: …… Name: ……..

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER B.TECH DEGREE EXAMINATION (S), MAY 2022
ELECTRONICS AND COMMUNICATION ENGINEERING
(2020 SCHEME)

Course Code: 20ECT203

Course Name: Logic Circuit Design

Max. Marks: 100 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Convert 125.625 into binary and octal.
2. Find the value of G where $(900)_8 = (240)_G$.
3. State and prove De-Morgan's Theorems.
4. Find the Max term of the Boolean function F= (A+B'+C) (B'+C)(A'+B').
5. Write the Verilog code of a full adder.
6. Implement a half adder using NAND gate.
7. Draw a four bit Ring counter with its state diagram.
8. Compare sequential and combinational circuits.
9. Compare the performance of TTL and CMOS logic families.
10. Define noise margin.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Do the following arithmetical operation
    i. $65.75_{(8)} - 46.56_{(8)}$
    ii. $9AB.26_{(16)} + 6CD.64_{(16)}$ (8)
    iii. $1101.11_{(2)} * 101.1O_{(2)}$
    iv. $1110_{(2)} / 101_{(2)}$
    b) Define keywords, modules, operators of Verilog HDL. (6)

OR

12. a) i) Represent (– 37.75) in floating point.
    ii) Represent 624 in BCD and Excess 3 Code. (7)
    b) Explain various data types and statements in verilog. (7)

MODULE II

13. a) Design a combinational circuit using the simplified expression of the given Boolean function using K Map and implement it using basic gates (8)
    $F(A,B,C,D)=\pi M(2,8,9,10,11,12,14)$
    b) Write the verilog code for the reduced expression of the above function (6)

OR

14. a) Simplify the given Boolean function using K Map and implement it using basic gates. (8)

$$f(A, B, C, D) = \sum m(0.1,2,4,5,8,9,10,12,13)+d\ (3,6)$$

b) Write the verilog code for the reduced expression of the above function. (6)

MODULE III

15. a) Design a 2 bit magnitude comparator and implement it using gates. (10)

b) Write verilog code for 8:3 encoder. (4)

OR

16. a) Design a multiplexer to realize the function represented by

$F (A, B, C, D) = \sum m (0,1,2,3,5,7,8,9,10,12,13)$, using

i) 16:1 MUX

ii) 8:1 MUX

iii) one 8:1 MUX (9)

b) Write Verilog code for 8:1multiplexer. (5)

MODULE IV

17. a) Design a SR flip flop from JK flip flop. (8)

b) With a neat diagram explain the working of a 2 bit synchronous up counter. (6)

OR

18. a) Design a Mod 10 asynchronous down counter. (8)

b) Write truth table and excitation table of JK flip flop and derive the characteristic equations. (6)

MODULE V

19. a) Explain the working of TTL NAND gate Totempole configuration with a neat diagram. (8)

b) Describe the working of CMOS inverter with a neat diagram. (6)

OR

20. a) Explain the working of CMOS NOR gate with a neat diagram. (8)

b) With relevant illustrations, describe the working of TTL inverter. (6)

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