Register No.: …… Name: ……..

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER B.TECH DEGREE EXAMINATION (S), MAY 2022
COMPUTER SCIENCE AND ENGINEERING
(2020 SCHEME)

Course Code: **20CST203**

Course Name: **Logic System Design**

Max. Marks: **100** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Show the three different binary representations (in 8 bits) for the decimal number -68.
2. Convert $(163.875)_{10}$ to a) binary b) octal and c) hexadecimal number systems.
3. Express the function, f(A, B, C) = AB' + BC in product of Maxterms form.
4. Using K- Map simplify the function F(w, x, y, z) = Σ (0, 1, 3, 4, 5, 6, 7, 13, 15) .
5. Implement a full adder using half adders.
6. Write the truth table of a 1 x 4 demultiplexer and show the corresponding logic diagram.
7. Give the truth table, characteristics table and excitation table of SR flip-flop.
8. How is a sequential circuit different from a combinational circuit? Give an example for each circuit.
9. The value of a float type variable is represented using the single-precision 32-bit floating point format IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A float type variable X is assigned the decimal value of −85.125. What is the representation of X in hexadecimal notation?
10. How is *static RAM* different from *dynamic RAM*?

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Find the 12-bit 2's complement form of the following decimal numbers
    i) -97.5 (4)
    ii) -73.0625
    b) Subtract the following octal numbers by a) 7's complement arithmetic b) 8's complement arithmetic (10)
    i) 256 – 643
    ii) 243.6 – 705. 64

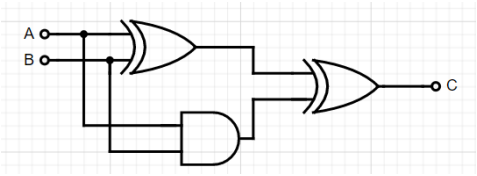
OR

12. a) If √61 = 7, find the base of the number system. (4)
    b) Perform the following operations in 8 bits using a) 1's complement representation b) 2's complement representation (10)
    i) (-35) + (-19)

ii) (+68.75) – (-27.25)

MODULE II

13. a) Redraw the circuit given after simplification



(4)

b) Using Quine- McClusky method of tabular reduction, minimize the given combinational single output function, f(A, B, C, D) = ∑ (2, 3, 8, 10, 12, 13, 14). (10)

OR

14. a) Simplify the given logic expression using K-map and implement the real minimal expression in universal logic. (10)
F(A, B, C, D) = π (1, 4, 5, 11, 12, 14) . d (6, 7, 15)

b) Reduce the given Boolean expression, (4)
F(X, Y, Z) = XY + (XZ)' + XY'Z (XY + Z)

MODULE III

15. a) Design and implement a 2-bit magnitude comparator (7)

b) Design a combinational circuit that accepts a 3-bit BCD number and generates an output binary number equal to the square of the input number. (7)

OR

16. a) Design a code converter for converting binary to Gray code (7)

b) Implement the following Boolean function using a 8X1 multiplexer and additional gates as needed (7)
f(A, B, C, D) = Σ(1, 3, 4, 11, 12, 13, 14, 15).

MODULE IV

17. a) What is race around condition? Why does it occur? Discuss how master-slave flip-flop eliminates it. (7)

b) Design a type D counter that goes through the states 0, 1, 2, 4, 0, …. The unused states must always go to zero (000) on the next clock pulse. (7)

OR

18. a) How to convert a J-K flip flop to S-R flop? Show conversion table, K-map and logic diagram. (7)

b) Design a Mod-6 asynchronous counter using T flip flops. Also verify its operation by means of a timing diagram. (7)

MODULE V

19. a) Implement the following Boolean functions using a 3×4×2 PLA (7)
F1 = Σ (0, 1, 3, 4)
F2 = Σ (1, 2, 3, 4, 5)

b) Illustrate the algorithm for addition and subtraction two binary numbers in signed magnitude form. (7)

OR

20. a) Implement a 4- bit bidirectional shift register with parallel load. (7)

b) Illustrate the algorithm for addition and subtraction of two floating point numbers. (7)

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