Register No.: ..... Name: .....

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER M.TECH DEGREE EXAMINATION (Regular), FEBRUARY 2022

(VLSI & Embedded Systems)

(2020 Scheme)

Course Code : 20ECVET231

Course Name: Computer Architecture and Parallel Processing

Max. Marks : 60 **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Compare UMA and NUMA models of parallel computers.
2. Discuss in brief on the advent of multithreading in processors design.
3. Write short notes on VLIW processors.
4. Why is branch prediction algorithm needed? Differentiate between static and dynamic techniques.
5. Compare the two different cache write policies.
6. Write short notes on cache coherence issues.
7. Write short notes on the models of memory consistency.
8. Describe CMP processor architecture with suitable diagram.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

9. Discuss in detail on Flynn's taxonomy of computer architecture with suitable diagrams. (6)

OR

10. Describe about data flow architectures with an example. (6)

MODULE II

11. Discuss in detail on superscalar processor organization with neat diagram? (6)

OR

12. Consider an application where floating-point (FP) instructions are responsible for 40% of execution time and floating-point square root (FPSQR) instructions take 15% of execution time. Compare the two designs given below. (6)
    Design A: FP instructions faster by 3 times
    Design B: FPSQR instructions faster by 15 times

MODULE III

13. Assume that a non-pipelined processor has a 1 ns clock cycle and it uses 4 cycles for ALU operations and branches and 5 cycles for memory operations. Also, assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose that due to clock skew and setup, pipelining the processor adds 0.2 ns of overhead to the clock. Ignoring any latency impact, how much speedup in instruction execution rate will gain from a pipeline. (6)

OR

14. Discuss in detail on the concept of Register Renaming and justify how it exploits ILP? (6)

MODULE IV

15. Differentiate between Direct mapping and Set Associative mapping with suitable illustrations (6)

OR

16. Elaborate on the various memory technologies and its relevance. (6)

MODULE V

17. Give a brief idea on cache coherence issues and discuss on the protocols for enforcing cache coherence. (6)

OR

18. Consider a 2-level cache system and calculate its average memory access time (AMAT) with the following specifications: Level 1 cache hit time=1 cycle and its miss rate= 3%, Level 2 cache hit time=7 cycles and miss rate=19%, Level 2 cache miss penalty= 110 cycles. (6)

MODULE VI

19. What is hardware multithreading? Compare and contrast fine grain multithreaded and coarse grain multithreaded systems. (6)

OR

20. Write in detail on Buses and Crossbar switch interconnection networks for parallel systems. (6)

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