Register No.: …… Name: ……..

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

THIRD SEMESTER B.TECH DEGREE EXAMINATION (Regular), FEBRUARY 2022
ROBOTICS AND AUTOMATION
(2020 SCHEME)

Course Code: **20RBT205**

Course Name: **Digital Electronics**

Max. Marks: **100** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Perform arithmetic operation (**15 – 4**) using 2's complement system. Use 8 bits for each number including sign bit. Express result in binary form.
2. (i) Find the gray code of following binary number : 11010101
   (ii) Convert the following gray code into its binary: 10101110
3. Determine the standard sum of products (SOP) form of the logic expression:
   F (A, B, C, D) = AB + A'BD' + BC'D
4. Realize a full adder using two half adders.
5. What are the asynchronous inputs of a flip flop and discuss its functions?
6. List the applications of shift registers.
7. Distinguish between asynchronous and synchronous counters.
8. What is meant by accuracy, linearity and resolution of D/A Converter?
9. Compare static RAM and dynamic RAM.
10. Write a Verilog code for NAND gate.

PART B

(Answer one full question from each module, each question carries 14 marks)

MODULE I

11. a) Two numbers A & B in Hex are given: A = 85CA, B =23C6
    (i) Find the decimal equivalent of A & B
    (ii) Find the binary of A & B
    (iii) What is the sum of A & B in binary? (6)

    b) With a neat diagram of TTL NAND gate, explain its operation. What is meant by sourcing and sinking? (8)

OR

12. a) Convert $(2AC5.D)_{16}$ to decimal, octal and binary. (6)

    b) Define the terms noise margin, propagation delay, fan in and power dissipation of logic families. Compare TTL and CMOS logic families showing the values of above-mentioned terms. (8)

MODULE II

13. a) Minimize the following Boolean function using K map: $F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$. Realize the circuit using basic logic gates. (8)

b) Explain the working of a ripple carry adder with the help of a diagram. (6)

OR

14. a) Describe decoders using suitable examples. Design a BCD to decimal decoder. (6)

b) With necessary diagrams, explain the working of an 8:1 Multiplexer and a 1:8 Demultiplexer. (8)

MODULE III

15. a) Define race-around condition. How is it eliminated? Illustrate with the help of necessary sketches. (8)

b) Realize a JK flip flop using SR flip flop. (6)

OR

16. a) Draw a 4-bit Serial In Parallel Out shift register and explain its working. (6)

b) Design a MOD-12 asynchronous counter (ripple counter) using JK flip flop. Explain the working with truth table and timing diagram. (8)

MODULE IV

17. a) Design the circuit of a 4-bit Johnson's counter. Show the timing signals also. (4)

b) Design a synchronous counter using T Flip Flop to count the following sequence 0 – 3 – 4 – 6 – 0. (10)

OR

18. a) Explain the operation of successive approximation ADC with neat diagrams. (5)

b) With neat diagrams, explain the operation of R-2R ladder DAC. Determine the resolution of (a) 6-bit DAC (b) 12-bit DAC in terms of percentage. (9)

MODULE V

19. a) Implement the following functions using PLA.
$F_1 = \Sigma m (3,5,7)$
$F_2 = \Sigma m (4,5,7)$ (7)

b) Draw the structure of a 16 x 4 ROM. (7)

OR

20. a) Differentiate between PROM, PAL and PLA. (9)

b) Write the Verilog code for a full adder circuit. (5)

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