

Register No.: ..... Name: .....

**SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)**

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

**FIRST SEMESTER M.TECH DEGREE EXAMINATION (Regular), FEBRUARY 2022***(VLSI & Embedded Systems)***(2021 Scheme)****Course Code :** 21VE102**Course Name:** Advanced Digital Design**Max. Marks :** 60**Duration: 3 Hours****PART A***(Answer all questions. Each question carries 3 marks)*

1. Define Essential Prime Implicants with an example.
2. Draw the Mealy state diagram for 010 overlapping sequence detector.
3. Draw the logic circuit for the following Boolean function.  $F = AB' + BC$ . Analyze the possibility of static 1 hazard in the circuit.
4. Draw ASM chart for the function  $Y = A + BC$ .
5. Draw the circuit of a 4-bit up counter.
6. Draw the High-Level State Diagram for a Soda Dispensing system.
7. Define Latency and Throughput.
8. Write the Verilog HDL code for a 16 bit register as part of a laser-based distance measuring system data path.

**PART B***(Answer one full question from each module, each question carries 6 marks)***MODULE I**

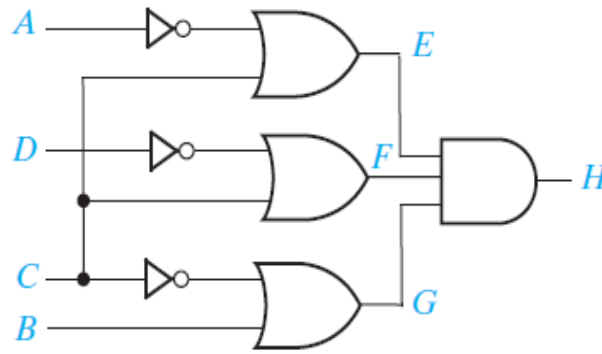
9. Draw the Mealy State Diagram and State Table of sequence detector to detect input sequences 0101 or 1001. The circuit resets after every four inputs. (6)

**OR**

10. Draw the logic circuit of a synchronous decade counter and write down the Verilog HDL code for it. (6)

**MODULE II**

11. For the circuit shown in the figure assume the inverters have a delay of 1 ns and the other gates have a delay of 2 ns. Initially  $A = B = C = 0$  and  $D = 1$ ; C changes to 1 at time 2 ns. Draw a timing diagram and identify the transients that occur. Modify the circuit to eliminate the hazards, if any. (6)



**OR**

12. Using an example describe the method of avoiding critical races in a circuit. (6)

**MODULE III**

13. Design a 4 input register with 2 control inputs s0 and s1; 4 data inputs i0,i1,i2,i3; and 4 data outputs q0,q1,q2,q3; When s1s0=00,the register maintains its value. When s1s0=01, the register set its outputs to 1111 value. When s1s0=10, the register shifts the data right by one bit. When s1s0=11, the register loads its inputs. (6)

**OR**

14. Design an ALU with two 8-bit inputs A and B, and control inputs x, y, and z. The ALU should support the operations described in table. Use an 8-bit adder and an arithmetic/logic extender.

Inputs			Operation
x	y	z	
0	0	0	S = A - B
0	0	1	S = A + B
0	1	0	S = A * 8
0	1	1	S = A / 8
1	0	0	S = A NAND B (bitwise NAND)
1	0	1	S = A XOR B (bitwise XOR)
1	1	0	S = Reverse A (bit reversal)
1	1	1	S = NOT A (bitwise complement)

(6)

**MODULE IV**

15. Create a data path for a laser-based distance measuring system from its HLASM. (6)

**OR**

16. What is the significance of Microprogrammed control unit in microprocessor design? Explain few control signal generations. (6)

**MODULE V**

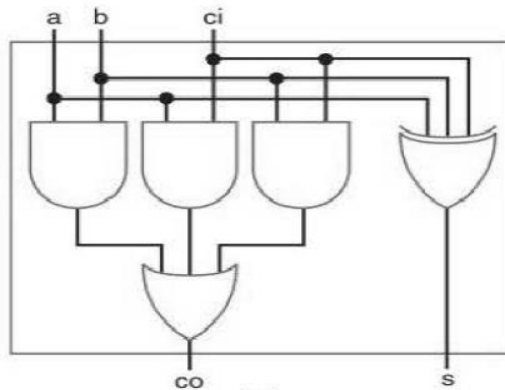
17. Convert the following C-like code, which calculates the greatest common divisor (GCD) of the two 8-bit numbers a and b, into a high-level state machine. (6)  
 Inputs: byte a, byte b, bit go  
 Outputs: byte gcd, bit done

```

GCD:
while(1) {
    while(!go);
    done = 0;
    while ( a != b )
        {
            if( a > b ) {
                a = a - b;
            }
            else {
                b = b - a;
            }
        }
    gcd = a;
    done = 1;
}
    
```

**OR**

18. A 4-bit carry-ripple adder is designed using the full adder circuit shown in the figure. Assume all gates have a delay of 2 ns. Determine the critical path for the 4-bit carry-ripple adder in the following conditions (a) wires have no delay, (b) wires have a delay of 1 ns.



(6)

**MODULE VI**

19. For each of the following functions, find all of the prime implicants using the Quine McCluskey method.  
 $f(a, b, c, d) = \Sigma m(2, 4, 5, 6, 9, 10, 11, 12, 13, 15)$ . Realize the optimized logic circuit. (6)

**OR**

20. Describe the RTL design optimizations and trade-offs. (6)

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