Register No.: …… Name: ……..

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FIRST SEMESTER M.TECH DEGREE EXAMINATION (Regular), FEBRUARY 2022

(VLSI & Embedded Systems)

(2021 Scheme)

Course Code : **21VE104-E**

Course Name: **ASIC Design and Verification**

Max. Marks : **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Describe the program structure of Verilog.
2. List out three low power techniques employed in modeling of state machine using Verilog.
3. Explain interface in System Verilog.
4. What is bus functional model and state its advantages.
5. Explain the two types of interfaces in UVM factory.
6. Differentiate blocking and unblocking interface in TLM.
7. List out the advantages of UVM sequence.
8. Describe the importance of objection mechanism in UVM model.

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

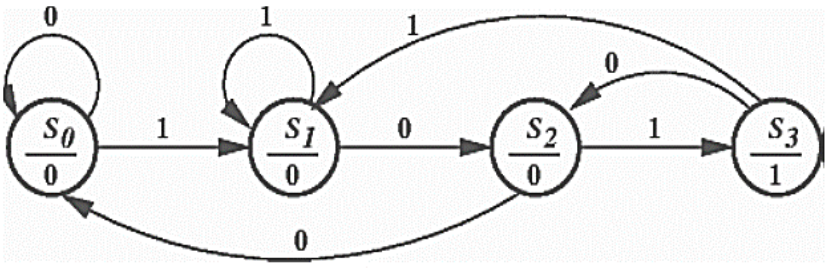
9. Design an up/down counter in Verilog. (6)

OR

10. Implement the SOP Y= AB+BC'+AD. (6)

MODULE II

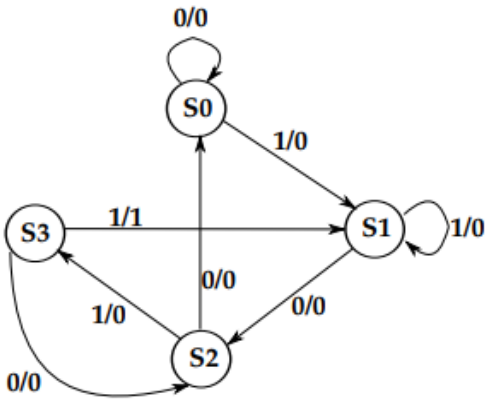
11. Implement a Moore machine in Verilog.



(6)

OR

12. Write the Verilog code for the following Mealy FSM shown in Fig. (6)



MODULE III

13. Distinguish between Queue and Stack in System Verilog. (6)

OR

14. Explain about System Verilog Mailbox. (6)

MODULE IV

15. Explain in detail about SV assertions with suitable examples. (6)

OR

16. Differentiate code coverage and functional coverage. (6)

MODULE V

17. Describe the sequence of common phases which are executed in UVM. (6)

OR

18. Describe the components of a Testbench. (6)

MODULE VI

19. Explain the connection and components of RAL with Testbench. (6)

OR

20. Illustrate UVM RAL model. State its advantages (6)

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