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SAINTGITS COLLEGE OF ENGINEERING
KOTTAYAM, KERALA
(AN AUTONOMOUS COLLEGE AFFILIATED TO
APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

FIRST SEMESTER M.TECH. DEGREE EXAMINATION (R), MARCH 2021
VLSI AND EMBEDDED SYSTEMS

Course Code:	20ECVET105
Course Name:	CMOS VLSI DESIGN
Max. Marks:	**60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

1. Distinguish Switching and Short circuit power dissipation in CMOS inverter.
2. Illustrate logical effort with an example.
3. Summarize the working of CMOS based NOR gate with circuit diagram.
4. Realize CMOS SR latch circuit based on NOR2 gate.
5. Realize NOR and NAND gates using Pseudo-NMOS logic.
6. Interpret DCVS logic with an example.
7. Illustrate NORA CMOS logic circuit with an example.
8. Interpret zipper CMOS circuits.

PART B

(Answer one full question from each module, each question carries 6 marks)
MODULE I

9.   Illustrate Noise margin of an Inverter. Demonstrate the equation for perturbed output   (6)
     of the Inverter.

OR

10. What are the sources of power dissipation in a CMOS inverter? Derive the expression   (6)
     for dynamic power dissipation

MODULE II

11. Illustrate the RC delay model of a CMOS inverter. Derive the expression for fall and   (6)
     rise delay.

OR

12. Discuss the logical effort of two input NAND and NOR gate.   (6)

MODULE III

13. Illustrate the implementations of AOI and OAI gates using CMOS logic with an example? (6)

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OR

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14. Realize the Boolean function $Y = \overline{(A + B + C)(D + E)(F+G)}$ in CMOS logic. (6)

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MODULE IV

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15. Implement and explain the operation of D latch using CMOS implementation with necessary waveforms? (6)

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OR

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16. Analyze the operation of a clocked SR latch using CMOS with necessary timing diagram. (6)

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MODULE V

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17. Illustrate the working of two input AND gate using pass transistor logic. Explain the requirement of level restorer circuit in pass transistor logic? (6)

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OR

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18. Give a comparison between NMOS, Pseudo NMOS and CMOS logic with the help of an INVERTER example. (6)

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MODULE VI

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19. Discuss different types of NORA CMOS logic with its circuit diagram and operation? (6)

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OR

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20. Implement the given function in dynamic CMOS logic and Domino CMOS logic. (6)

$$Z = AB + \overline{BC} + \overline{C}$$

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