Register No.: …… Name: ……..

SAINTGITS COLLEGE OF ENGINEERING (AUTONOMOUS)

(AFFILIATED TO APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY, THIRUVANANTHAPURAM)

SECOND SEMESTER INTEGRATED M.C.A DEGREE EXAMINATION (S), December 2021

Course Code: **20IMCAT106**

Course Name: **INTRODUCTION TO DIGITAL SYSTEMS & LOGIC DESIGNS**

Max. Marks: **60** **Duration: 3 Hours**

PART A

(Answer all questions. Each question carries 3 marks)

		CO
1.	Convert $(110101)_2$ and $(111001)_2$ to Decimal.	[1]
2.	Convert $(100011110101)_2$ to hexa decimal number.	[1]
3.	Implement AND gate using NOR gate	[2]
4.	Prove A(A+B)=A	[2]
5.	Write short note on T flip flop.	[3]
6.	Convert to Standard SOP ABD+ACD+BCD	[3]
7.	Draw the circuit diagram of 2 to 4 decoder	[4]
8.	Explain 2 bit comparator with an example.	[4]
9.	Give details about serial-in serial-out shift register.	[5]
10.	Compare synchronous and asynchronous counters.	[5]

PART B

(Answer one full question from each module, each question carries 6 marks)

MODULE I

		CO	Marks
11.	Represent -45 in 8-bit sign magnitude, 1's complement and 2's complement form.	[1]	(6)

OR

		CO	Marks
12.	Do the following : a. 10110 + 1001 b. 1110 - 111 c. 10110 * 101	[1]	(6)

MODULE II

		CO	Marks
13.	Describe basic gates in detail.	[2]	(6)

OR

		CO	Marks
14.	State and prove Demorgan's Theorem.	[2]	(6)

MODULE III

		CO	Marks
15.	Minimize the Boolean Expression $f(A,B,C,D)=\Sigma\{0,2,3,4,5,6,8,10,11,12,13,14\}$.	[3]	(6)

OR

		CO	Marks
16.	Explain JK-flip flop in detail.	[3]	(6)

MODULE IV

		CO	Marks
17.	Design a full adder.	[4]	(6)

OR

		CO	Marks
18.	With a diagram explain 4x1 Multiplexer.	[4]	(6)

MODULE V

		CO	Marks
19.	Discuss the working of Parallel-In Serial-Out shift register.	[5]	(6)

OR

		CO	Marks
20.	Design a 3 bit synchronous counter.	[5]	(6)

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