Reg. No._____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SECOND SEMESTER MCA (REGULAR) DEGREE EXAMINATION, MAY 2017

Course Code: RLMCA112

Course Name: COMPUTER ORGANIZATION AND ARCHITECTURE

Max. Marks: 60 Duration: 3 Hours

PART A

Answer All Questions, Each Carries 3 Marks

1. Differentiate big-endian and little-endian assignments of byte addressable memory.
2. Show how a stack can be implemented using auto-increment and auto-decrement addressing modes?
3. Write the sequence of control steps required for single bus organization for add the (immediate) number NUM to register R1.
4. What is WMFC? Why is the WMFC step needed when reading from or writing to main memory?
5. What is meant by Bus arbitration?
6. List the difference between DRAM and SRAM.
7. What is memory interleaving? What is the change obtained in access time with interleaving?
8. Define Set associative Cache.

PART B

Answer Any One Question from Each Module. Each question carries 6 Marks.

MODULE I

9. With a neat diagram explain the operational concepts of a computer.

OR

10. What are the functional units of a computer?

MODULE II

11. Define addressing modes. Classify and explain with example.

OR

12. With neat diagram describe input and output operations?

MODULE III

13. Differentiate between hardwired and micro programmed control units?.

OR

14. With neat diagram describe the working of a single bus organization

MODULE IV

15. Describe the hardware mechanism for handling multiple interrupt requests.

OR

16. What is the need for input output interface? Explain the functions of a typical 8-bit parallel interface.

MODULE V

17. a) Explain the terms memory latency and bandwidth.

    b) A main memory constructed with SDRAM chips that have 2 clock cycles for selecting a row and 1 cycle for placing first set of bits in data line, expect that the burst length is 8 .If 32 bits of data are transferredin parallel and 133 MHz Clock is used, hoe much time does it required to transfer i) 32 bytes of data ii) 64 bytes of data. What is the latency in each case?

OR

18. Explain about different ROM memories.

MODULE VI

19. How the virtual address is converted into real address in a paged virtual memory system? Explain.

OR

20. A block- set associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words.

    a) How many bits are there in a main memory address?

    b) How many bits are there in each of the TAG, SET and WORD fields?

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